Prof. Feras Hamdan Al-Hawari

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Education

PhD in Electrical and Computer Engineering, June 2007
Northeastern University, Boston, Massachusetts, USA

MS in Computer Engineering, June 1995
Florida Institute of Technology, Melbourne, Florida, USA

BS in Electrical and Computer Engineering, June 1993
Jordan University of Science and Technology, Irbid, Jordan

Work Experience

- **German Jordanian University**, Amman, Jordan (September 2021 - Current)

***Dean**, School of Electrical Engineering and Information Technology*: Lead the efforts in the school to establish the B.Sc. in Design and Media Informatics program jointly with the School of Architecture and Built Environment at GJU. Besides, the Artificial Intelligence & Machine Learning as well as the Computer Vision and Robotics tracks were established in the B.Sc. in Computer Engineering (CE) program. Also, the Cyber Security as well as the Data Science tracks were established in the B.Sc. in Computer Science (CS) program. Moreover, the Internet of Things (IoT) track was established in the Electrical Engineering (EE) program. Furthermore, a Dual Study track was established in the B.Sc. in CS as well as the B.Sc. in CE programs. An agreement with Huawei is being finalized to integrate practical courses in security and 5G technologies in the study plans of the CE, CS, and EE undergraduate programs.

- **German Jordanian University**, Amman, Jordan (September 2021 - Current)

***Director**, University Digitalization Project*: Continue the leadership of the team to digitalize the academic and business processes at GJU through architecting, analyzing, designing, developing, testing, and deploying state-of-the-art student and enterprise information systems (see roles at ISTC below).

- **German Jordanian University**, Amman, Jordan (February 2021 - Current)

***Professor**, School of Electrical Engineering and Information Technology*.

- **German Jordanian University**, Amman, Jordan (February 2017 - February 2021)

***Associate Professor**, School of Electrical Engineering and Information Technology*.

- **German Jordanian University**, Amman, Jordan (January 2012 - September 2021)

***Director**, Information Systems and Technology Center (ISTC):* Founder of the software development division in the center (now under university digitalization project). Project manager and technical lead for the ERP tools development projects. Participated in the analysis, design, development, testing, and deployment of the student information system (MyGJU), revenue system, e-fawateercom services, financial system, payroll system, HR system, online exams system, voting system, helpdesk system, information display system, and supplies system. Directed, and contributed to, the IT efforts to transition the instruction at GJU to fully online during the corona virus crisis period. Managed, and participated in the specification of, the following IT projects: GJU website, Moodle deployment, smart classrooms, network infrastructure, data center, IP cameras and surveillance system, VoIP telephony framework and video conferencing system. Established a workshop in the center to maintain data shows, copiers, and computers. Educated, mentored, and motivated the employees in the center. Enhanced the confidence, inter-personal skills, and collaboration skills of the team. Filled the gaps in the following IT areas: software development, website development, database design/administration, Linux administration, cloud services, and e-learning services. Prepared the yearly budget for the center and evaluated the performance of all employees on a yearly basis.

- **German Jordanian University**, Amman, Jordan (September 2011 - February 2017)

***Assistant Professor**, School of Electrical Engineering and Information Technology*.

- **Cadence Design Systems**, Chelmsford, MA, USA (September 1995 - September 2012)

Senior Member of Consulting Staff *in the Silicon Package Board (SPB) High Speed R&D group*: Technical lead for the circuit simulation technology group that focused on: signal integrity (SI) analysis of high-speed PCBs and packages; flows and methodologies to validate source synchronous and serial interfaces such as DDR3 and PCI-Express respectively; topology exploration; circuit building and simulation; interconnect and s-parameters modeling; behavioral I/O device (e.g. IBIS, AMI) modeling; model translation; constraints management; measurements, waveforms display; results reporting; and SI tools integration.

- **Computer Interactive Technology**, Atlanta, Georgia, USA (Summer 1995)

Network Administrator: Built and managed a Novell local area network (LAN). Assembled each PC, installed the Novell NetWare software on the PCs, linked the PCs with Ethernet cables, and configured and managed the user as well as email accounts.

- **Florida Institute of Technology**, Melbourne, Florida, USA (August 1994 - May 1995)

Assistant System Administrator: Assisted students in the VAX-VMS computer laboratory and opened and managed their computer accounts.

- **Jordan University of Science and Technology**, Irbid, Jordan (Fall 1993)

Teaching Assistant: Taught the Motorola-68000 interfacing laboratory; designed and prepared the experiments; monitored and assisted the students; and conducted and corrected the exams.

- **Computer City**, Irbid, Jordan (Summer 1992)

Summer Intern: Built and maintained custom desktop PCs.

Publications

PhD Thesis:

- Feras Hamdan Al-Hawari, "Application-level QoS management system for network computing," PhD Thesis. ECE Department, Northeastern University, Boston, USA, April 2007.

USA Patents:

- Feras Al-Hawari, Terry Jernberg, and Roger Cleghorn, "System and method for automatic correction of flight time skew of timing signals in simulated source synchronous interface operation", U.S. Patent 9,542,512, issued January 10, 2017.
- Jose Schutt-Aine, Dennis Nagle, Feras Al-Hawari, Ambrish Varma, Jilin Tan, Ping Liu, Shangli Wu, Yubao Meng, Qi Zhao, and Zhongyong Zhou, "System, method, and computer program product for input/output buffer modeling", U.S. Patent 9,460,250, issued October 4, 2016.
- Taranjit Kukal, Feras Al-Hawari, Dennis Nagle, Raymond Komow, and Jilin Tan, "System and method for implementing power integrity topology adapted for parametrically integrated environment", U.S. Patent 8,656,329, issued February 18, 2014.
- Feras Al-Hawari, Taranjit Kukal, Dennis Nagle, Raymond Komow, and Jilin Tan, "System and method for adapting behavioral models to fluctuations in parametrically integrated environment", U.S. Patent 8,452,582, issued May 28, 2013.
- Feras Al-Hawari, Jilin Tan, and Jose Schutt-Aine, "Method and system for adaptive modeling and simulation of lossy transmission lines", U.S. Patent 8,386,216, issued February 26, 2013.
- Taranjit Kukal, Feras Al-Hawari, Dennis Nagle, Raymond Komow, and Jilin Tan, "System and method for adapting electrical integrity analysis to parametrically integrated environment", U.S. Patent 8,286,110, issued October 9, 2012.
- Ambrish Varma and Feras Al-Hawari, "Method and system for screening nets in a post-layout Environment", U.S. Patent 8,060,852, issued November 11, 2011.

Best Paper:

- Robert Blake, Phil Murray, and Feras Al-Hawari, "Challenges in implementing DDR3 memory interface on PCB systems: A methodology for interfacing DDR3 SDRAM DIMM to an FPGA", CDNLIVE! EMEA, Silicon-Package-Board Co-design Track, Munich, Germany, May, 2008.

Journals:

- Feras Al-Hawari, "Software design patterns for data management features in web-based information systems", Journal of King Saud University - Computer and Information Sciences, https://doi.org/10.1016/j.jksuci.2022.10.003, 2022.
- Feras Al-Hawari, Hala Barham, Omar Al-Sawaeer, Mai Alshawabkeh, Sahel Alouneh, Mohammad I Daoud, and Rami Alazrai, "Methods to achieve effective web-based learning management modules: MyGJU versus Moodle", PeerJ Computer Science, 7:e498, DOI:10.7717/peerj-cs.498, 2021.
- Feras Al-Hawari, Mohammed Al-Sammarraie, and Taha Al-Khaffaf, "Design, validation, and comparative analysis of a private bus location tracking information system", Journal of Advanced Transportation, 2020(8895927), pp. 1-18, 2020.
- Feras Al-Hawari, Mai Al-Zu'bi, Hala Barham, and Wael Sararhah. "The GJU website development process and best practices", Journal of Cases on Information Technology, IGI Global, 23(1), pp. 1-24, 2020.
- Feras Al-Hawari, "Holistic university website management: people, technology and processes", TEM Journal - Technology, Education, Management, Informatics, 9(4), pp. 1771-1779, 2020.
- Feras Al-Hawari and Mohammad Habahbeh. "Secure and robust web services for e-payment of tuition fees", International Journal of Engineering Research and Technology, 13(7), pp. 1795-1801, 2020.
- Rami Alazrai, Amal Al-Saqqaf, Feras Al-Hawari, Hisham Alwanni, and Mohammad I. Daoud. "A time-frequency distribution-based approach for decoding visually imagined objects using EEG signals", IEEE Access, Vol. 8, pp. 138955–138972, 2020.
- Daoud, M., Abdel-Rahman, S., Bdair, T., Al-Najar, M., Al-Hawari, F., and Alazrai, R., "Breast tumor classification in ultrasound images using combined deep and handcrafted features", Sensors, 20(23), pp.1-1, 2020.
- Feras Al-Hawari, Mahmoud Al-Ashi, Fares Abawi, and Sahel Alouneh. "A practical three-phase ILP approach for solving the examination timetabling problem", International Transactions in Operational Research, 27(2), pp. 924-944, 2020.
- Feras Al-Hawari. "Automatic and multithreaded method for determining the number of vector fitting poles based on empirical data", International Journal of Numerical Modelling Electronic Networks Devices and Fields, John Wiley, 32(2), e2512, 2019.
- Feras Al-Hawari, Mai Alshawabkeh, Haytham Althawbih, and Omar Abu Nawas. "Integrated and secure web-based examination management system", Computer Applications in Engineering Education, John Wiley, 27(4), pp. 994-1014, 2019.
- Feras Al-Hawari and Hala Barham. "A machine learning based help desk system for IT service management", Journal of King Saud University - Computer and Information Sciences, Elsevier, DOI: 10.1016/j.jksuci.2019.04.001, 2019.
- Sahel Alouneh, Feras Al-Hawari, Ismail Hababeh, and Gheorghita Ghinea. "An effective classification approach for big data security based on GMPLS/MPLS networks", Security and Communication Networks, Hindawi, vol. 2018, Article ID 8028960, 10 pages, 2018.
- Feras Al-Hawari, Anoud Alufieshat, Mai Alshawabkeh, Hala Barham, and Mohammad Habahbeh, "The software engineering of a three-tier web-based student information system (MyGJU)", Computer Applications in Engineering Education, 2(25), pp. 119-133, 2017.
- Feras Al-Hawari, "Analysis and design of an accounting information system", International Research Journal of Electronics and Computer Engineering, 3(2), pp. 16-21, 2017.
- Feras Al-Hawari, "MyGJU student view and its online and preventive registration flow", International Journal of Applied Engineering Research (IJAER), 1(12), pp. 119-133, January, 2017.
- Jose Schutt-Aine, Patrick Goh, Yidnekachew Mekonnen, Feras Al-Hawari, Jilin Tan, Ping Liu, and Wenliang Dai, "A comparative study of convolution and order reduction techniques for blackbox macromodeling using scattering parameters", IEEE Transactions on Components, Packaging and Manufacturing Technology (IEEE-TCPMT), 10(1), pp. 1642-1650, October, 2011.

- Patrick Goh, Jose Schutt-Aine, Demetri Klokotov, Jilin Tan, Ping Liu, Wenliang Dai, and Feras Al-Hawari, “Partitioned latency insertion method with a generalized stability criteria”, IEEE Transactions on Components, Packaging and Manufacturing Technology (IEEE-TCPMT), 9(1), pp. 1447-1455, September, 2011.

Conference Papers:

- Feras Al-Hawari, Khaled Tayem, Sahel Alouneh, and Anass Al-Ksasbeh, “Methodology to evaluate the performance of Hadoop MapReduce on a Hyper-V cluster using SAN storage”, The International Arab Conference on Information Technology (ACIT'2022), IEEE, Abu Dhabi, UAE, 2022.
- Sahel Alouneh, Ala' Khalifeh, Dhiah el Diehn I. Abou-Tair, and Feras Al-Hawari, "An open source LoRaWAN simulator framework for the Internet of Things applications", 8th International Conference on Internet of Things: Systems, Management and Security (IOTSMS), 2021.
- Feras Al-Hawari, Hadi Etaiwi, and Sahel Alouneh, "A cost effective information display system based on open source technologies", International Conference on New Trends in Computing Sciences (ICTCS 2017), pp. 277-282, Amman, Jordan, October 11-13, 2017.
- Feras Al-Hawari, "Analysis and design of an accounting information system", 7th International Research Conference on Science, management, and Engineering, Dubai, UAE, 2017.
- Sahel Alouneh, Ismail Hababeh, Feras Al-Hawari, and Tamer Alajrami, "Innovative methodology for elevating big data analysis and security", The 2nd International Conference on Open Source Software Computing (OSSCOM 2016), pp. 1-5, Beirut, Lebanon, December 1-3, 2016.
- Jose Schutt-Aine, Jilin Tan, Ping Liu, Feras Al-Hawari, and Ambrish Varma, "IBIS modeling using latency insertion method (LIM)", 16th IEEE Workshop on Signal Propagation and Interconnects (SPI), pp. 97-100, Sorrento, Italy, 13-16 May, 2012.
- Patrick Goh, Jose Schutt-Aine, Demetri Klokotov, Feras Al-Hawari, Jilin Tan, Ping Liu, and Wenliang Dai, “Partitioned Latency Insertion Method (PLIM) with stability considerations”, 15th IEEE Workshop on Signal Propagation and Interconnects (SPI), pp. 107-110, Italy, May, 2011.
- Jose Schutt-Aine, Demetri Klokotov, Patrick Goh, Jilin Tan, Feras Al-Hawari, Ping Liu, and Wenliang Dai, "Application of the latency insertion method to circuits with blackbox macromodel representation", 11th IEEE Electronics Packaging Technology Conference (EPTC09), pp. 92-95, Singapore, December, 2009. (Invited Paper)
- Jose Schutt-Aine, Feras Al-Hawari, Jilin Tan, and C. Kumar, “Blackbox macromodel with S-parameters and fast convolution”, IEEE Workshop on Signal Propagation and Interconnects (SPI-08), pp. 1-4, Avignon, France, May, 2008.
- Feras Al-Hawari, “S-parameter based multi-conductor transmission line modeling and simulation”, Cadence Technical Conference, Anaheim, California, May, 2008.
- Phil Murray and Feras Al-Hawari, “Challenges in implementing DDR3 memory interface on PCB systems: a methodology for interfacing DDR3 SDRAM DIMM to an FPGA”, DesignCon 2008, Santa Clara, California, February, 2008.
- Feras Al-Hawari, “Fast time domain analysis of frequency dependent data using the direct convolution with approximation approach”, Cadence Technical Conference, Monterey, California, April, 2005.
- Jilin Tan, Feras Al-Hawari, and Dragoslav Milosovic, “Via modeling in multi Gbits/s signal analysis”, Association for Computational Electromagnetic Society (ACES), Albany, New York, 2004.
- Feras Al-Hawari and Jilin Tan, “S-parameter based wideband simulation technology on digital circuit boards”, Cadence Technical Conference, San Jose, California, May, 2003.
- C. Kumar and Feras Al-Hawari, “Template oriented software design”, Cadence Technical Conference, Napa Valley, California, May, 1996.

Demonstrations:

- Kent Drumstad, Adge Hawes, Taranjit Kukal, Feras Al-Hawari, Ambrish Varma, and Terry Jernberg, "Supporting external circuit as spice or s-parameters in conjunction with I-V/V-T tables", Asian IBIS Summit, Yokohama, Japan, November 2011.
- Feras Al-Hawari, "Setup and analysis of DDR2 source synchronous memory interfaces in Allegro PCB SI", Cadence Technical Conference, Keystone, Colorado, May 2007.
- Feras Al-Hawari, "A demo for s-parameters transient simulation support in SigXP", Cadence Technical Conference, San Jose, California, April 2004.

Posters:

- Elias Manolakos, Demetris Galatopoullos, and Feras Al-Hawari, "MATLAB and Java integration for distributed image processing applications", Communications and Digital Signal Processing Center, Northeastern University, March 2008.
- Feras Al-Hawari, "A method for SPICE-level transient simulation of digital PCB structures characterized by S-parameters", Cadence Technical Conference, San Jose, California, April 2004.

White Papers:

- Feras Al-Hawari and Elias Manolakos, "Application-aware middleware to support runtime component self-adaptation strategies in cluster computing", Electrical and Computer Engineering Department, Northeastern University, Boston, USA, 2008.
- Feras Al-Hawari and Elias Manolakos, "Middleware to support self-adaptation of components for fault tolerance in network computing applications," Electrical and Computer Engineering Department, Northeastern University, Boston, USA, 2008.
- Feras Al-Hawari and Elias Manolakos, "Startup-phase QoS management system and an efficient mapping heuristic for network computing applications", Electrical and Computer Engineering Department, Northeastern University, Boston, USA, April 2006.
- Feras Al-Hawari and Elias Manolakos, "Performance engineering of coarse grain network computing applications", Electrical and Computer Engineering Department, Northeastern University, Boston, USA, April 2005.

Other Publications:

- Feras Al-Hawari, "Help: JavaPorts Visual Task Composer (JPVTC)", Electrical and Computer Engineering Department, Northeastern University, Boston, MA, 2006.
- Feras Al-Hawari, "Help: QoS GUI", Electrical and Computer Engineering Department, Northeastern University, Boston, MA, 2006.
- Feras Al-Hawari, "Help: QoS service and middleware for runtime adaptation and application fault tolerance", Electrical and Computer Engineering Department, Northeastern University, Boston, 2006.
- Feras Al-Hawari, "Tutorial: constructing network application models using JavaPorts tools", Electrical and Computer Engineering Department, Northeastern University, Boston, MA, 2006.

Capacity Building Projects

- *International Master of Science on Cyber Physical Systems* **(MS@CPS)**. GJU Investigators: Dhiah Abou Tair, Sahel Alouneh, Ala Khalifeh, Samer Nofal, and Feras Al-Hawari. Erasmus+ program - Key Action 2 - Capacity Building in the Field of Higher Education, European Commission. Period: 1/11/2018-31/10/2021.
- *Jordan Opportunity for Virtual Innovative Teaching and Learning* **(JOVITAL)**. GJU Investigators: Dr. Mohammad Daoud, Dr. Sahel Alouneh, Dr. Rami Alazrai, and Dr. Feras Al-Hawari. Erasmus+ program - Key Action 2 - Capacity Building in the Field of Higher Education, European Commission.
- *A Bottom-up Approach for Opening up Education in South-Mediterranean Countries* (**OpenMEd**). GJU Investigators: Mohammad Daoud, Manar Fayyad, Salem Al-Agtash, Loay Salhieh, Rana Sabri, Sahel Alouneh, and Feras Al-Hawari. Erasmus+ program - Key Action 2 - Capacity Building in the Field of Higher Education, European Commission. Period: 1/10/2015-30/9/2018.

Awards

The German Jordanian University Award of Excellence (2016) for establishing the software development team as well as architecting and participating in the development of the student information system (MyGJU), accounting system, and financial system.

Courses Taught

- Computing Fundamentals
- Computing Fundamentals Lab
- Digital Systems Design Lab
- Electrical Circuits I
- Electrical Circuits II
- Electrical Circuits I & II Labs
- Systems Programming
- Systems Programming Lab
- Object Oriented Programming
- Object Oriented Programming Lab
- Software Design and Architecture
- Advanced Software Analysis and Design
- Senior Project I & II
- Master Thesis (Supervisor)

GJU related Committees

- Member in GJU Deans Council
- Chair of the SEEIT School Council
- Chair of the SEEIT Research Council
- Chair of the SEEIT Graduate Studies Council
- Chair of the SEEIT Dual Studies Committee
- Chair of the SEEIT Marketing Committee
- Member in the Dual Studies University Committee
- Member in the Dual Studies Revision Committee
- Member in the Registration Procedures Committee
- Member in the Admission Requirements Committee
- Member in the Committee to review the study plans of the new B.Sc. programs at GJU
- Member in GJU Staff Mobility Program (SMP) Selection Committee
- Member in the Technical Advisory Committee at the Jordanian Universities Network (JUNET)
- Member in the University Emergency Committee
- Member in the MOHE E-Learning Committee
- Member in the MOHE Priorities Implementation Committee
- Member in the Digital Teaching Strategy Steering Committee
- Chair of the Digital Teaching Strategy Technical Committee
- Member in the Coronavirus Committee
- Member in the Online Exams Guidelines Committee
- Member in the ITG Case Committee
- Member in the Managers Committee
- Member in the E-Learning Committee
- Member in the Similar Courses Committee
- Member in the Students Elections Committee
- Member in the Central Tenders Committee
- Member in the Employees Committee
- Member in the Students Disciplinary Board
- Member in the Inventory and Stocking Committee

- Member in the University Budget Committee
- Member in the ERP Tools Evaluation Committee
- Member in the Quality Assurance and Accreditation Committee
- Member in the Data Center Migration Committee
- Member in the committees to accept the following projects: network infrastructure, IP cameras and surveillance system, data center, and video conferencing system.
- Member in the Computer Engineering Department Scientific Research Committee
- Member in the Comprehensive Exam (for the Master in CE program) Committee
- Member in a Master Thesis Defense Committee
- Member in several Senior Project Defense Committees

Miscellaneous Activities in the USA

- Associate Editor for the IEEE Transactions on Components, Packaging and Manufacturing Technology (IEEE-TCPMT) journal (2012-Current).
- Active member in the IBIS advanced technology modeling (IBIS-ATM) task group that exists to develop and promote a system for modeling advanced electronic interfaces, with a current emphasis on SerDes-based designs (2009-2012).
- Lead researcher in a joint research project between *Cadence* and *University of Illinois at Urbana-Champaign* (represented by Prof. Jose E. Schutt-Aine) that focuses on transient simulation techniques and model order reduction methods for passive and non-linear circuits (2005-2012).
- Interacted closely with companies like *Micron*, *Altera*, and *Celestica* to architect an SI analysis flow for source synchronous memory interfaces (e.g., DDR2, DDR3) in Allegro PCB SI (2005-2012).
- Participated in a project between *Cadence* and *IBM* to integrate some of their point tools (e.g., PowerSpice simulator, CZ2D field solver) within the Allegro Package/PCB SI tools, 2006.
- Member in a project between Cadence and *Intel* that focused on methods for efficient transient simulation techniques for passive structures characterized by S-Parameters, 2002.
- Member in the Technical Program Committee, Cadence Technical Conference, California, 2006.
- Served as reviewer for several academic journals and conferences such as: the IEEE transactions on advanced packaging; the IEEE international conference on acoustics, speech, and signal processing (ICASSP); IASTED international conference on parallel and distributed computing and systems (PDCS); Computer Applications in Engineering Education (Wiley CAE); and Journal of King Saud University - Computer and Information Sciences (Elsevier).
- Consulting on various areas related to the SpecctraQuest and SigXP tools (2000-2012).

ERP Tools and Website Development at GJU

- In February 2014, Dr. Feras Al-Hawari was entrusted by the GJU President Prof. Natheer Abu Obeid and the Deans Council at GJU to establish, manage, and train a software development team at GJU to develop in-house the university ERP tools and website. Moreover, **his academic load was reduced to three credit hours each semester** so he can participate in the design and development of the tools, given his long experience in the USA software industry.
- Dr. Al-Hawari founded, and is leading, a team that is comprised of himself (as a project manager, architect, system analyst, database analyst, database designer, Java EE developer, and tester), nine software engineers, one website developer, and one database administrator.
- Dr. Al-Hawari trained the software engineers by having them attend his following courses: Object Oriented Programming (in which they learned Java), Software Design and Architecture (in which they learned Java EE, design patterns, as well as database analysis and design), and Systems Programming.
- Dr. Al-Hawari and the system administration team in the center specified the hardware requirements (server machines, storage, network switches, firewalls, cabinets, etc.) for the new data center that will host the Java EE application servers and DBMS servers. In addition, they

agreed to use Linux as an OS to run all machines. Moreover, hardware and software security plans/measures were implemented to secure the servers and applications from cyber-attacks.

- Dr. Firas Al-Hawari decided to develop the applications based on a three-tier web-based architecture. Accordingly, HTML, JSF, Ajax, JavaScript, and PrimeFaces elements as well as CSS files were used to develop the client tier. The Java programming language and Java EE APIs were used to develop the application logic (beans, models, and DAOs) in the web (application) tier with Glassfish used as an application server. While the Oracle DBMS was used to manage the database tables in the business (data) tier. In addition, the NetBeans IDE and SQL Developer were used for application and database development and design respectively. Moreover, GIT and Source Tree were used for version control.
- Dr. Al-Hawari adopted the project management (project plan, project progress, review meetings, version control, risk management, and disposal plan) and software development processes in the ISO/IEC 29110 systems engineering basic profile to manage and develop the various projects. Whereas Dr. Al-Hawari and his team used the iterative and incremental software development process (methodology) to develop the various software systems.
- Most of the needed systems were successfully delivered in record time and with high quality. The system measurements data and user survey results illustrated that the delivered systems are feature rich, easy to use, fast, reliable, stable, available, and scalable. By the end of July 2022, Dr. Al-Hawari and his team were able to analyze, design, develop, test, and deploy the following web-based applications:
    1) **University Website (December 2014)**: Dr. Al-Hawari was the manager of this project, as well as the architect of the website infrastructure, content structure, and graphical design. The team produced a website that is simple, nice looking, easy to navigate, well structured, content rich, and dynamic. The graphic design of the website is being renewed now (2022).
    2) **Financial System (March 2015)**: It is mainly used by the finance department staff to manage financial accounts, budgets, and cost centers. It also enables managing the following system setup information: user accounts, user privileges, financial accounts tree, currencies, departments, banks, cost centers, reserve funds, and petty cash. Besides, it facilitates the management of university budgets, department budgets, financial transactions (e.g., payment vouchers, receipt vouchers, and journal vouchers), and financial bookings. Furthermore, it allows the generation of various financial reports (e.g., budget levels, trial balance, journal ledger, transactions, checks and bookings reports) that can be evaluated by higher management to evaluate and improve the financial situation for the university.
    3) **Student Information System MyGJU (September 2015)**: This system has three views:
        - **Student View**: Allows students view their personal, academic and financial information, as well as add/drop course sections during the registration period. They can view their course portfolios (e.g., objectives, learning outcomes, syllabus, assessment, and materials), schedules, attendance, grades, study plans, and transcript. In addition, they may use the tuition fees calculator as well as view their financial statement of account to decide whether to deposit any money in their accounts ahead of registration. Furthermore, they can evaluate their instructors and courses to help the GJU administration assess the performance of the faculty members and enhance the educational process based on their valuable feedback.
        - **Instructor View**: Enables instructors to view their personal information, schedules, grades and evaluations, as well as search all the offered course sections in a selected academic semester. Additionally, instructors can manage, enter, and submit the grades of the students in their course sections. Furthermore, advisors, chairs and deans may view the academic information (e.g., personal information, study plans, schedules, grades, transcripts, holds, and financial information) of their students to monitor their academic progress and to provide them with the needed academic advising. Whereas, the deans/chairs may also monitor the registration status, manage (add, edit, view and delete) course sections, view study plans, and view the instructor grades and evaluations of their schools/departments respectively.

- **Administrator View**: Lets registrars at the GJU manage the MyGJU system and student information. As part of the system and academic setup tasks the registrars may manage user details, buildings, rooms, countries, faculties, departments, courses, requisite courses, equivalent courses, study plans, course sections, and prerequisite tests. Moreover, they can use the admission flow to fill the student admission applications as well as reject or accept students. Besides, they can transfer students to different majors or change their programs. Furthermore, the registrars manage the student personal information, substitute courses, transfer credit, holds, and notes. Additionally, they can perform add, drop, and withdraw course section transactions on behalf of the students. They can also view the student or instructor schedules, grades, or evaluations. In addition, they are responsible for posting the grades to the transcripts and computing the GPA and status for all students. They can find the expected to graduate students, graduating students, and issuing certificates to the graduates. Finally, MyGJU provides the registrars with powerful capabilities to generate various reports for statistical, archiving, and administrative purposes.

4) **Accounting System (September 2015)**: This system is fully integrated with MyGJU and allows accountants to perform the following tasks: manage tuition and services fees; define sponsors and scholarships; link students to scholarships; upload bank payments; manage student exemptions; manage student financial accounts; and generate registration invoices. Additionally, an accountant may carry out the following operations on a student account: view student information (e.g., personal information, study plan, academic status, grades, transcript, holds, financial exemptions, major transfers, and scholarships), view schedules, view registration invoices, manage statement of account, and record accounting transactions (e.g., payments, refunds, balance adjustment, scholarship payments, scholarship refunds, and opening balances). Moreover, the accountants can generate various reports to monitor income, expenses, student balances, and sponsor balances as well as track all transactions and generate statistical data to analyze and improve the accounting procedures at the GJU.
5) **Information Display System (August 2016)**: This system was developed and deployed to allow displaying announcements, news, slideshows, and other information on LED TV screens that are mounted in different public locations (e.g., lobbies, squares, hallways, and cafeterias) at the GJU campus. A dynamic web page application was developed to display the information on the screens. In addition, a content management application (CMA) was implemented to allow system administrators to use their computers (or other devices) to remotely manage (add, edit, view, and delete) the displayed content.
6) **E-Fawateercom Service (August 2016)**: The students may use this service to instantly deposit money (via E-Banking) in their MyGJU accounts from the comfort of their homes. Consequently, when MyGJU receives an online banking payment it will instantly account for its amount in the corresponding student's account balance in MyGJU, which may immediately cover the cost of the tuition fees for the course sections that the student desires to add during the registration period.
7) **Human Resources and Payroll System (December 2016)**: It enables the HR department staff to manage university levels, entity types (e.g., school, deanship, department, and center), university entities (e.g., specific schools and departments), commission types (e.g., manager, vice, and staff), job titles (e.g., director, accountant, computer engineer, and technician), countries, health insurance contracts, tax laws, as well as employee types (academic or administrative), classifications, categories, grades, and grade categories. Whereas it allows the finance department staff to manage salary slip items, salary slip templates, basic salaries, incentives, deduction types, allowance types, as well as university, administration, transportation, specialization, personal, GJU, rarity, residence, and extra allowances. In addition, it lets the system administrators search for an employee, add a new employee, as well as edit and view an employee's basic information. Furthermore, they can manage (i.e., add, edit, view, and delete) the employee's detailed information such as certificates, experiences, family members, commissions, status, banks accounts, telephones, health

insurance, leaves, vacations, deductions, allowances, and salary setup. Besides that, the system is used to compute the monthly salaries and generate the respective salary slips for all employees. Moreover, the system can be used to generate various reports to help the staff of the HR and finance departments in their daily and end of year work and analysis. Further, the system supports the online management of vacations, leaves and fingerprint for all administrative employees.

8) **Voting System (December 2016)**: This simple system was developed in-house to enable the GJU students to elect their representative to the university council.
9) **Online Examination Management System (September 2017)**: The web-based examination management system allows defining and setting up exams according to a flexible tree-based exams structure. Moreover, it integrates a rich text editor for composing exams suitable for different engineering and language disciplines. In addition, it automates the scheduling, grading and reporting processes in order to relieve instructors from such cumbersome tasks. Furthermore, its capabilities and integration with different databases enable it to offer several security schemes that support strong multifactor authentication and authorization, detect impersonation and prevent cheating. Besides, it provides an easy to use and informative wizard that enables students to take exams.
10) **Help Desk System (February 2018)**: The help desk system acts as a single point of contact between users and IT staff. It also utilizes an accurate ticket classification machine learning model to associate a help desk ticket with its correct service from the start and hence minimize ticket resolution time, save human resources, and enhance user satisfaction. Further, it supports an administrator view that facilitates defining offered services, administering user roles, managing tickets and generating management reports. Also, it offers a user view that allows employees to report issues, request services, and exchange information with the IT staff via help desk tickets. Moreover, it supports automatic email notifications amongst collaborators for further action. Yet, it helps in defining business processes with well-defined activities and measuring KPIs to assess the performance of IT staff and processes.
11) **Course Weekly Schedule and Files Folder in MyGJU (February 2019)**: This module allows defining course information such as description, objectives, learning outcomes, references, and exam assessments. Furthermore, each course section has a page where instructors add learning materials and activities for their students. The page is organized week by week, and the system automatically generates one div for each week in an academic semester. Consequently, an instructor can post relevant tasks, notes, references, and files within each week's div. Also, the files can be either posted to the week div from the instructor's computer or from the shared folder of the course (i.e., reused). Each course is associated with a folder to be used by instructors for uploading, sharing, and organizing the course materials (e.g., slides, exercises, quizzes, homework, notes, and videos).
12) **Publications Flow in MyGJU (February 2019)**: The publications flow allows instructors to manage (add, edit, and view), and import (via a Crossref web service), their publications for archiving and other future purposes (e.g., automatic generation of promotion forms).
13) **Student Attendance (July 2019):** This module provides a flexible student attendance management flow that automatically builds the attendance days based on the course section schedule as well as the semester period; allows taking attendance for multiple days at once; supports various attendance states (i.e., present, absent, late, official excuse, and private excuse); and flags student attendance violations for further action (e.g., failing the student in the course).
14) **Guests Portal (July 2020):** This system allows prospective students to submit (online) applications for admission to all academic programs offered by the university at the undergraduate and graduate levels. It allows managing the admission applications electronically, including filling the personal information of the student, entering the data of the high school certificate, uploading the required documents and certificates, in addition to choosing the required majors. Each account is also linked to an electronic payment number

that permits a student to pay the application fee electronically via the E-Fawateercom service through the e-banking channels of all Jordanian banks.

15) **Course Withdrawal Flow in MyGJU (2021).**
16) **Substitute Courses Flow in MyGJU (2022).**
17) **Seat Reservation Flow in MyGJU (2022).**
18) **Supplies System (Expected January 2023).**

- Dr. Al-Hawari is also responsible for administering (e.g., monitoring server health and logs) the application server, as well as testing and then deploying all applications updates. Moreover, he participates in the administration of the database, and is responsible for executing all the SQL scripts that are needed to alter or update either the structure of, or data in, the database tables as well as to add new database tables.

Online Teaching/Assessment at GJU Due to Coronavirus Crisis Ramifications

In response to the coronavirus crisis ramifications, Dr. Al-Hawari and his ISTC team worked 24/7 for several months to support fully online teaching/assessment at GJU during the second 2019/2020 semester. Some of the taken measures in that regard are:

- Evaluated the MS Office 365 tools (which were made available by ISTC to all GJU users since 2017) to recommend the most suitable/reliable/secure solutions for online teaching. Accordingly, ISTC recommended: MS Teams for live and interactive lecture streaming/recording; Skype for Business for live video conferencing; MS Stream for video archiving; the Moodle LMS for electronic quizzes/exams; MyGJU as a learning management system (course portfolio, lectures, video links, attendance, grades, evaluation, emails, etc.); OneDrive for file storage; Outlook for email; and MS office tools like Word, PowerPoint, OneNote, and Whiteboard for authoring.
- Prepared specifications for all the devices (e.g., desktops, laptops, tablets, mics, cams, printers, etc.) to be used in online teaching.
- Launched an e-learning website to provide links to various video (and other) tutorials to help the GJU staff prepare and deliver online content.
- Worked with the e-learning committee to prepare many video tutorials related to the supported platforms and the online teaching scenarios.
- Produced various tutorials related to the supported online exam types (i.e., handwritten/typewritten exams, electronic multiple-choice exams, and oral exams).
- Prepared, configured, fine-tuned, secured, and tested the Moodle servers to allow many (more than 1000 users) concurrent users to perform online quizzes and exams.
- Provided technical support during many exams and quizzes to resolve issues and provide tips.
- Supported an electronic signature service to allow instructors to electronically sign documents online for the continuity of the administrative processes.
- Provided 24/7 support to instructors and students regarding the tool usability and accounts.
- Made sure all the needed services, tools, and infrastructure are highly available for the continuity of the online teaching process.
- Organized a webinar, in coordination with the e-learning committee, to solicit the instructor's feedback and answer their questions regarding the online teaching experience for improvement purposes.
- Specified the hardware/software requirements for 15 smart classrooms to support online and interactive learning at the GJU, the team then received and launched the rooms in 2021.

Research and Development at Cadence Design Systems

- 17 years of experience in the software development cycle from the product requirement, functional and design specification to the development, testing, and maintenance phases.
- Technical lead for the circuit simulation technology, which includes a SPICE-based simulation engine (Tlsim) that is used in the Allegro Package/PCB SI tools to perform AC/DC as well as transient circuit analysis. My tasks were focused on maintaining and enhancing the simulator, as well as setting up the future direction for the simulation technologies within the SPB High Speed group. Some of my contributions in this area are:
  1. Modeling and transient simulation of passive circuit elements characterized by frequency dependent data such as impedance (Z), admittance (Y), and scattering (S) parameters. Implemented three methods to support that:
     a) *Direct convolution method*: This is based on calculating the *impulse response* of the system (using the Inverse Fast Fourier Transform *IFFT*) and then using *direct convolution* to find the time domain currents/voltages at the system ports. In addition, the *passivity* of the model is checked and guaranteed. Moreover, the *Hilbert transform* is used to enforce the *causality* of the response.
     b) *Fast convolution method*: A state of the art method that reduces the complexity of the direct convolution method from $O(N^2)$ to $O(N\log(N))$, where N is proportional to the number of time steps in each simulation.
     c) *Macro-modeling method*: This is the fastest method, and it has a $O(N)$ complexity. It is based on using the *vector fitting method* to obtain a pole/residue (partial fraction) representation (transfer function) of the passive element and then generating *state-space models* or *indirect convolution* formulas to obtain the *MNA* matrix stamps and then the transient response.
  2. Modeling and transient simulation of *transmission lines* characterized by frequency dependent RLGC data based on a method that uses the following techniques: (1) *split S-Parameters*, (2) *delay extraction*, (3) *vector fitting and partial fraction representation*, and (4) *state-space model formulation*.
  3. Investigated the *Latency Insertion Method* (LIM) for fast transient simulation.
  4. Maintaining and enhancing the transient simulation code for the rest of the supported elements in Tlsim such as the non-linear *IBIS* (I/O Buffer Information Specification) models, *W-Element* based transmission line models, diodes, voltage and current controlled sources, and lumped elements (e.g., R, L, C, K).
  5. Maintaining the SPICE parser, matrix package, and the waveform generation code.
- Led a group of 5 engineers to architect and develop a post-route analysis flow to setup and validate source synchronous interfaces (e.g., Dual Data Rate DDR memory interfaces) in the Allegro PCB SI tool (SpecctraQuest). The flow supports the following features.
  1. *Interface setup*: Identify the controller from the SDRAM components. Define the data, address, and control buses. Associate the buses with their corresponding strobe/clock signals. Assign Pseudo Random Bit Patterns (PRBP) to the address/data buses. Specify the On Die Termination (ODT) programmability of the controller and SDRAMs when they are receiving, driving, or in stand by mode.
  2. *Analysis and simulations*: Perform comprehensive analysis to account for reflection, xtalk and simultaneous switching noise (SSN) effects. Automatically simulate the buses for all possible ODT, drivers and receivers combinations as well as IO buffers process, voltage, and temperature (PVT) variations.
  3. *Measurements and reports*: Measure and report worst-case timing (e.g., setup/hold times and margins) and distortion (e.g., noise margin, overshoot, undershoot) values. Adjust the setup and hold times based on the measured slew rate of the data/clock signals as well as user defined derating tables. Display the eye diagrams of the various signals.
- Integrated the Intel Math Kernel Library (MKL) in the circuit simulator (Tlsim) to enable the automatic parallelization of the matrix algorithms on multi-core processors.

- Designed and implemented an open software framework (GUI work, model templates, infra-structure work, netlist translators, waveform translators, measurement, and reporting code) that enables the use of third-party simulators (e.g., HSPICE, Spectre, PowerSpice) and their device models in the Cadence pre- and post-route Allegro PCB SI tools (e.g., SigXplorer, SpeecctraQuest). This framework allows designers to simulate a PCB with complex I/O models (structural and transistor-based models) that cannot be represented in IBIS-style format (behavioral and I/V and V/t-based models). In addition, it allows designing ICs and PCBs concurrently. The architecture was recently extended to allow using other third-party engines (e.g., 2D and 3D field solvers) in the Cadence tools.
- Maintained and enhanced the SpecctraQuest circuit building code. This code generates SPICE netlist files for a selected net or group of nets in the PCB. These files are then passed to the circuit simulator to analyze the PCB. This code retrieves the buffer models that are assigned to the driver/receiver pins of the selected net from the device library. In addition, it invokes the field solver to obtain the electrical models (i.e., RLGC data, S-Parameters) for the passive structures (e.g., traces, vias) that constitute the net. Moreover, it applies the required stimulus to the corresponding nodes based on the desired analysis type (e.g., reflection, xtalk, SSN). Finally, it connects all the electrical models together and generates the corresponding SPICE netlist files for the whole circuit.
- Participated in the design of the S-Parameter generation flow in SigXplorer. This flow allows the designer to generate an S-Parameter blackbox for a given topology that consists of passive elements (e.g., transmission lines, S-Parameters, vias, capacitors, resistors, mutual inductors). An AC frequency sweep is used to generate the S-Parameters.
- Worked on the measurement and reporting code. The measurement code calculates timing (e.g., switch, settle, setup, and hold times) and distortion (e.g., overshoot, noise margins) values based on the simulated waveforms. The measured values are stored in an internal database (simulation cache) and then displayed in a summary report.
- Designed the GUI, data structures, and C/SKILL database APIs for the device modeling libraries (DML) and interconnect modeling libraries (IML) in SpecctraQuest.
- Wrote an API to compare the physical information (geometry) of the IML models (e.g., traces and vias). The circuit builder uses this API to check if an electrical model for a given geometry is already solved and stored in the IML library. If the model is found in the library it will be retrieved and used by the circuit builder without resolving it, otherwise the field solver will be invoked to obtain the model and store it in the IML library for future reference.
- Implemented code to save all the used device models in the Allegro database. In addition, I developed a GUI to compare and synchronize the saved model data with the corresponding data in the DML library.
- Worked on various translators such as *ibis2signoise* (translates IBIS to DML format), *spc2spc* (translates Tlsim netlist to HSPICE or Spectre netlist), and *ts2dml* (translates touchstone to DML format). In addition, I worked on the dmlcheck program, which checks the syntax of a DML file and the validity of the contained models.
- Implemented a GUI to invoke the s2ibis program in order to convert a structural I/O model (transistor-level SPICE circuit) to a behavioral IBIS model (IV and VT curves representation).
- Worked with SWATH connectors, packaged devices, and board models (EBD).
- Developed the design and net audit utilities, which are used to check if an Allegro PCB or net(s) are setup correctly to perform signal integrity (SI) PCB analysis.
- Implemented an MFC application to display stripline and microstrip transmission lines.
- Developed C-shell scripts to perform regression tests for the delivered features and tools.
- Ported the simulator and circuit builder code from UNIX to Windows.

PhD Research at Northeastern University

Dr. Feras Al-Hawari conducted his PhD research under the supervision of Prof. Elias Manolakos focusing on the development of an *application-level Quality of Service (QoS) management system for network computing* that: (1) automates the mapping of the tasks that form a network computing application to Networks of Workstations (NOWs) at *startup* time (i.e. before the application is launched), and (2) facilitates application-driven self-adaptation for performance (e.g., to balance the load) and fault tolerance (e.g., to overcome machine crashes) purposes at *runtime* (i.e. while the application is running). This work has been performed in the context of the JavaPorts project aiming at the development of a distributed components-based framework for heterogeneous network computing; and it consists of two main parts:

(1) Startup-phase QoS management framework to automatically map the application tasks onto a set of suitable machines. The major contributions of this part of the research are:

- An interactive QoS GUI and an underlying framework to allow the developer to run QoS management sessions to automatically, and quickly, identify a tasks-onto-machines mapping that may satisfy the desired QoS levels of a selected metric (e.g., application total execution time or speedup ratio) at *startup* time. The framework uses an efficient *mapping heuristic* to try to find an optimal mapping based on gathered *resources information* as well as *network and application models*. In addition, it uses a *performance estimation algorithm* to predict the overall execution time of the *best-found mapping* to determine if that mapping meets the desired QoS levels. The GUI is also used to: define the machines pool on which the application may run; deploy the *resources monitoring modules* on the defined machines to collect the machines and network links state information (to be used for application mapping and performance estimation purposes); manage and terminate the monitoring modules upon request; and display the resources information.
- A scalable and non-intrusive *resource monitoring system* to periodically measure and record the static/dynamic attributes of the *machines*, in a user defined pool, as well as the *network links* interconnecting them. The JavaPorts framework is used to launch a *monitoring module* on each machine in the pool. The modules are configured as a ring and the logical network links of the ring are used to exchange information between the various modules. The *JavaPorts message passing API* is used to send/receive the measured data and to pass a token to coordinate the monitoring events amongst the resource monitors. A *resource monitor* can obtain/measure the following *machine attributes*: number of CPUs on a machine, CPU speed, workload, free swap size, free RAM size, domain name, and OS type. In addition, it can accurately measure the *throughput* and *latency* of a network link at the application (RMI) and network (TCP/IP) levels. The throughput of a link is measured using two or four different message sizes to enable the system to *predict the throughput* of any message size.
- The *JavaPorts Visual Task Composer* (JPVTC) tool to graphically construct behavioral models for the application tasks and connect them structurally to build complete, two-level, hierarchical network computing (NC) application models. These models can be used for *performance engineering* and *rapid prototyping* of NC applications even before any code is developed. A behavioral task graph consists of nodes (elements) modeling basic code constructs and edges for defining the nodes execution ordering. It describes the general organization of a task as a sequence of computation and communication elements while abstracting low level details. Elements are annotated with attributes and benchmark data used in performance estimation. The tool allows modeling the following JavaPorts code constructs: sequential code blocks, iteration constructs (loops), conditionals (if statements), synchronous/asynchronous read/write message passing operations, spawning new threads. Furthermore, it saves the behavioral task graphs in an *eXtensible Markup Language* (XML) format defined in a graph *Document Type Definition* (DTD).
- An *efficient mapping heuristic* to map a computation and/or communication intensive distributed and multitasked application to the best available resources. The mapping is based on network and application representations as well as static/dynamic resources information.

- A *simulation-based performance estimation scheme* that uses the NC application models (constructed using the JPVTC tool) as well as the static/dynamic resources (e.g., network links, machines) state information (provided by the monitoring modules) to accurately predict the expected total running time of a given *distributed and multi-tasked* application configuration. The method can account for *execution*, *queuing*, and *synchronization delays* and can detect *potential deadlock* situations. It estimates *execution* and *queuing* delays by simulating a *time sliced scheduler* that inserts elements of multiple threads or tasks that contend for the same CPU into the same machine queue. Moreover, it mimics the way the JavaPorts communication port lists operate in order to account for the *synchronization* delays and model accurately the behavior of the supported *message passing operations*.
- A *clustering algorithm* to scale down the number of throughput measurements to be performed by the *resource monitoring modules*. The method is based on grouping (clustering) the machines that exhibit similar communication characteristics into one cluster. According to that the network of machines is represented as a simplified and fully connected clusters graph. Therefore, very few intra- and inter-clusters throughput measurements are needed to estimate the all-to-all communication delays between the machines in the pool.

(2) Runtime QoS Service and middleware to support application-driven self-adaptation for performance (e.g., to balance the load) and fault tolerance (e.g., to overcome machine and task failures). The major contributions of this part of the research are:

- Lightweight middleware to monitor at runtime the dynamically changing characteristics of the application tasks and of the system resources they use (i.e., machines and network links). The middleware monitors machine and task states (e.g., crashes) to provide services that enable JavaPorts tasks to self-adapt for fault tolerance in the case of machine or task failures. Furthermore, it measures machine attributes (e.g., CPU speed, workload, free RAM size) as well as network link throughput and latency to enable a task to balance the workload or react to link congestion by sending a job or a message to a peer task running on the machine with fastest CPU speed or over the network link with highest throughput respectively. To avoid any reliance on system-level middleware, the QoS middleware is tightly coupled with the application instance it is serving. Therefore, JavaPorts automatically launches and terminates the QoS middleware entities along with their companion network computing application. Furthermore, it configures these entities based on the structure of the tasks that form the application, which gives it the ability to launch only the proper monitors and collect only the data needed to maintain state information of the relevant resources.
- A simple to use and anonymous API that allows a task to retrieve different "views" of the measured attributes of the monitored application entities (tasks, machines, and links) and use them to make intelligent self-adaptation decisions to maintain specified application performance levels or circumvent task and machine failures, as needed. In an *anonymous* API the name (and port) of the destination task or machine does not need to be mentioned explicitly in any of its methods, which makes the application code independent from the underlying resources. Therefore, the application can be configured to run on a new set of machines without any need to modify its code. The API supports a set of methods that are commonly used for implementing applications that adapt for performance or fault tolerance. In addition, it supports a set of methods that enable the application to halt, resume, or change the behavior of the middleware at anytime. For example, when a task knows that it will not need any resource information for a while, it can avoid the monitoring overhead by halting the resource monitoring. Then, when the task knows that it may need the system state soon, it can resume the resource monitoring.

Computer Skills

- **Programming languages/analysis:** Java SE/EE, C#, C++, C, ADA, Pascal, FORTRAN, SKILL, MATLAB, assembly languages, OOA/OOD.
- **GUI development languages:** Java Swing, Visual C#, Visual C++, SKILL, JSF, JSP, PrimeFaces.
- **Network programming APIs:** Java/C TCP/IP API, Java RMI API.
- **Network protocols:** OSI reference model, Ethernet, Asynchronous Transfer Mode (ATM), SONET, TCP/IP, OSPF IGRP.
- **Hardware design languages:** VHDL.
- **Scripting Languages:** C-shell, JavaScript, and PHP.
- **Database languages/RDBMS/analysis:** SQL, Java Database Connectivity (JDBC), ADO.NET; Oracle, MySQL, MS SQL Server, MS Access; entity-relationship and fact-based database analysis as well as database normalization.
- **Database management/design/development tools:** Oracle SQL Developer, MySQL administrator, MS SQL server configuration manager, Navicat lite for MySQL, MySQL workbench, MS SQL studio management studio, MS Access.
- **Security:** Java Cryptology Architecture (JCA), Java Secure Socket Extension (JSSE), Java Authentication and Authorization Service (JAAS), Java keytool.
- **Development platforms:** Windows, UNIX, Linux, HP, AIX, MS-DOS, VAX/VMS.
- **Development/Debugging frameworks/tools:** Visual C++.NET, Visual C#.NET, Workshop, Visual C++ studio, NetBeans IDE 6.1, Forte for Java, dbx, purify, quantify.
- **Application/Web Servers:** Apache, Glassfish.
- **Circuit simulators:** Tlsim, HSPICE, PSPICE, Spectre, and SPICE3.
- **PCB/IC EDA design tools:** Cadence Allegro Package/PCB SI tools (SpecctraQuest, SigXplorer, Power Integrity, Model Integrity, Constraint Manager, Sigwave, Allegro Router, Advanced Package Designer), Cadence IC tools, Agilent ADS tools, SUPREM, VHDL tools.
- **Word processors:** MS Word, MS PowerPoint, LaTeX/TeX, Frame maker, vi.
- **Miscellaneous:** C#/Java multi-threading and collections, XML, DTD, USB specification, AMPL, SHARPE, Petri Net tools, Spice2IBIS, Clear Case, GIT, Source Tree, MS Excel, Visio, xfig, lex/yacc, cygwin, FrontPage, EndNote, DHTML

Graduate and Undergraduate Projects

- Developed a graphical tool (based on Java Swing/AWT) that uses the JDBC API to connect to a MySQL RDBMS in order to retrieve/display the data/metadata inside the user/system databases (this tool is similar to Navicat lite and MySQL administrator).
- Used a fact-based analysis approach to design a database to store information (names, phone numbers, addresses, emails, websites, notes, etc) about people and businesses of interest. The database tables were normalized to be in 5NF with referential/entity integrity constraints defined. Generated an ER diagram for the database and added it to the MySQL and SQL Server engines. Developed several stored procedures for the basic database operations. Implemented a GUI (using Visual C#) to allow a user to: connect to the database (using ADO.NET classes); insert (validate) new records into the database; find person/business information by name, phone, address, etc; update and delete selected database records.
- Designed and generated a database to store the USA zip codes with their corresponding city and state information. Populated the database with about 41000 valid tuples (zip code records) to be referenced by other databases.
- Used the Cadence IC tools to design a simple CPU. Performed the following design cycle steps: schematic capture, Design Rule Check (DRC), routing, simulation, and verification.
- Used the VHDL hardware design language to implement a CPU, RAM, ALU, and many other sequential as well as combinational circuits.
- Used SUPREM to design a simple CMOS transistor.

- Used PSPICE to design and verify many analog and digital electronic circuits (e.g., differential amplifiers, I/O buffers, rectifiers, and oscillators).
- Built a Motorola 68000 kit, interfaced it with a printer, a monitor, seven segment displays, RS232, and a kit for temperature and speed control. Wrote several assembly programs to control and test the kit.
- Wrote a program to simulate an 8-node network. Simulated the transmission of packets at the network, datalink, and physical layers.
- Developed a simple 6809 assembler.
- Implemented several static and dynamic mapping heuristics to schedule a class of independent jobs in a heterogeneous computing (HC) system (e.g., Opportunistic Load Balancing OLB, Minimum Completion Time MCT, K-Percent Best KPB).
- Developed various distributed applications based on the *Request* (self-scheduling) and *Assign* Manager-Worker programming paradigms.