

Feras Hamdan Al-Hawari, PhD

ACADEMIC LEADER | PROFESSOR | APPLIED RESEARCHER

Computer Engineering Department | School of Computing | German Jordanian University | Amman, Jordan

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Academic Leadership | Curriculum Innovation | Teaching and Supervision | Applied Research | Commercial Software R&D | University Digital Transformation

30+ years technology and engineering | Former Dean | 17 years U.S. R&D | 13+ years digital transformation | 7 U.S. patents

Academic Leadership Profile

Professor and former Dean combining academic leadership, teaching, and applied research with 30+ years of engineering experience. Electronic design automation R&D at Cadence Design Systems and ongoing university systems development enrich teaching, curriculum development, and student supervision. Connects theoretical foundations with engineering practice in software architecture, circuit simulation, and enterprise systems.

As Dean at German Jordanian University, renewed computing and engineering programs through emerging specializations, applied learning, and industry partnerships. Increased staffing, expanded facilities, and upgraded learning resources to support enrollment growth while strengthening teaching and assessment. Combines experience in university-wide academic decision-making with leadership of IT infrastructure and services.

Founded and continues to lead GJU's in-house software development capability, now the Digital Transformation Office, delivering integrated academic and administrative systems. This sustained effort has generated a substantial body of university systems research and underpins current AI initiatives in forecasting, decision support, and intelligent assistance.

Selected Academic and Institutional Impact

- **Led academic transformation and growth as Dean:** established a B.Sc. in Game Design and Media Informatics. Introduced undergraduate specializations in AI/ML, data science, computer vision, cybersecurity, and IoT, alongside Applied AI and AIoT master's tracks. Integrated EC-Council and Huawei curricula and certification pathways. Established Dual Study with three summer internships and promoted project-based learning. Program renewal and outreach helped triple enrollment. Doubled staffing, expanded facilities, upgraded equipment and software, and strengthened teaching and assessment. Directed school planning, budgets, and governance while contributing to university-wide academic decisions through the Deans Council.
- **Connect teaching and supervision with engineering practice:** draw on commercial software R&D and university systems development to teach programming, software architecture, systems programming, parallel computing, and electrical circuits. Connect theory with practical engineering examples, design decisions, and problem-solving. Extend this approach to supervision of master's theses and senior projects.
- **Established and continue to lead university digital transformation:** built a 13-member engineering team and delivered integrated ERP systems and a university portal. Prioritize digital transformation initiatives with university management and lead architecture, development, deployment, operations, and adoption. Previously directed university IT for nearly a decade, expanding infrastructure and digital-learning capabilities and leading the transition to fully online instruction during the pandemic.
- **Advance applied research and institutional AI enablement:** published research on university systems, big data, circuit simulation, and interconnect modeling. Apply machine learning and LLM/RAG to forecasting, decision support, and intelligent assistance, while working toward controlled agentic workflows. Serve as Associate Editor of *IEEE Transactions on Components, Packaging and Manufacturing Technology*.
- **Advanced EDA and circuit simulation at Cadence in the USA:** developed signal integrity analysis workflows with specialized DDR validation and third-party simulator integration. Led circuit simulation technology, enhancing the native simulator's models and algorithms for accuracy and efficiency. Combined technical leadership, hands-on development, and industry-university collaboration over 17 years, contributing to seven U.S. patents.

Academic and Professional Expertise

Academic Strategy and Governance • Curriculum Innovation • Teaching and Research Supervision • Applied Research • Industry Partnerships • Team and Capacity Development • Portfolio and Budget Management • University Digital Transformation • Enterprise Software and ERP Architecture • EDA and Circuit Simulation • AI and Data Analytics • IT Infrastructure and Cloud.

Education

- **PhD in Electrical and Computer Engineering**, June 2007

Northeastern University, Boston, Massachusetts, USA

- **MS in Computer Engineering**, June 1995

Florida Institute of Technology, Melbourne, Florida, USA

- **BS in Electrical and Computer Engineering**, June 1993

Jordan University of Science and Technology, Irbid, Jordan

Work Experience

- **German Jordanian University — Amman, Jordan (February 2021 – Present)**

Professor, School of Electrical Engineering and Information Technology.

- **German Jordanian University — Amman, Jordan (2013 – Present)**

Director, Software Development and Digital Transformation. *Successive mandates within ISTC (2013–2021), the Computerization Project (2021–early 2025), and the Digital Transformation Office (early 2025–Present):* Founded the university's in-house software development function, building and training a 13-member multidisciplinary team. Established its technical foundation, engineering standards, and delivery processes. Architected and continue to lead integrated ERP systems and the MyGJU portal spanning academic services, finance, revenue, electronic payments, HR, payroll, supplies, service management, correspondence, and archiving. Personally developed core components, reusable templates, and design patterns adopted across the team. Align project priorities with university management and stakeholder needs. Direct requirements analysis, design, development, quality assurance, functional and stress testing, deployment, and production operations. Coordinate infrastructure, cybersecurity, and operational readiness with IT. Lead documentation and employee training to support university-wide system use.

- **German Jordanian University — Amman, Jordan (September 2021 – 2025)**

Dean, School of Computing (formerly School of Electrical Engineering and Information Technology): Directed school strategy, governance, and resource planning. Contributed to university-wide academic policy and decisions through the Deans Council. Led a transformation culminating in the school's renaming to the School of Computing and threefold enrollment growth. Established the B.Sc. in Game Design and Media Informatics. Introduced Applied AI and AIoT tracks in the M.Sc. in Computer Engineering. Modernized undergraduate programs in Computer Engineering, Computer Science, and Electrical Engineering with specializations in AI/ML, Computer Vision, Data Science, Cybersecurity, and IoT. Integrated the Department of Basic Science (Mathematics and Physics) into the school. Promoted applied learning through project-based courses and student competitions. Established curriculum and certification partnerships with EC-Council and Huawei. Introduced Dual Study with internships at the same company across three consecutive summer semesters. Expanded recruitment through web updates, brochures, open houses, and outreach. Doubled academic and technical staffing, expanded facilities, and upgraded equipment and software to support growth and new programs. Improved teaching and assessment to uphold quality and meet student expectations.

- **German Jordanian University, Amman, Jordan (February 2017 - February 2021)**

Associate Professor, School of Electrical Engineering and Information Technology.

- **German Jordanian University, Amman, Jordan (January 2012 - September 2021)**

Director, Information Systems and Technology Center (ISTC): Led university IT strategy, operations, services, and continuity planning, managing budgets, resources, and staff performance. Built data-center, server, storage, network, cybersecurity, telephony, surveillance, conferencing, and digital-signage infrastructure. Established virtualized hosting, backups, and access controls supporting institutional systems and digital transformation. Oversaw email, Microsoft 365, and single sign-on. Advanced digital learning through Moodle, Teams, smart classrooms, and faculty support. Led the transition to online instruction during COVID-19. Set up a hardware maintenance workshop. Mentored the technical team across system and database administration, website management, cloud technologies, and e-learning.

- **German Jordanian University**, Amman, Jordan (September 2011 - February 2017)
Assistant Professor, School of Electrical Engineering and Information Technology.
- **Cadence Design Systems**, Chelmsford, MA, USA (September 1995 - September 2012)
Senior Member of Consulting Staff & Lead Software Engineer, Silicon-Package-Board High-Speed R&D Group:
Combined technical leadership with hands-on software engineering across the development lifecycle to advance Cadence's Allegro Package/PCB signal integrity (SI) tools. Developed pre-route and post-route SI analysis workflows with specialized DDR validation and third-party simulator integration. Contributions covered design capture, device and interconnect model libraries, translators, and analysis-specific circuit generation. Enabled consistent waveform measurement and reporting across simulators for timing and noise assessment. Led circuit simulation technology, advancing the native SPICE-based simulator's behavioral I/O and interconnect models, numerical algorithms, and multicore processing to improve accuracy and efficiency. Collaborated with industry partners and university researchers on simulation and modeling, contributing to seven U.S. patents.
- **Computer Interactive Technology**, Atlanta, Georgia, USA (Summer 1995)
Network Administrator: Architected and deployed a Novell Local Area Network (LAN) from the ground up, managing hardware assembly, physical Ethernet cabling, NetWare installation, and user and email account configuration.
- **Florida Institute of Technology**, Melbourne, Florida, USA (August 1994 - May 1995)
Assistant System Administrator: Managed VAX-VMS computer laboratory operations, providing technical support to students and overseeing account provisioning and administration.
- **Jordan University of Science and Technology**, Irbid, Jordan (Fall 1993)
Teaching Assistant: Instructed the Motorola-68000 interfacing laboratory, designed practical experiments, mentored students, and administered and graded course examinations.

Publications

PhD Thesis:

- Feras Hamdan Al-Hawari, "Application-level QoS management system for network computing," PhD Thesis. ECE Department, Northeastern University, Boston, USA, April 2007.

USA Patents:

- Feras Al-Hawari, Terry Jernberg, and Roger Cleghorn, "System and method for automatic correction of flight time skew of timing signals in simulated source synchronous interface operation", U.S. Patent 9,542,512, issued January 10, 2017.
- Jose Schutt-Aine, Dennis Nagle, Feras Al-Hawari, Ambrish Varma, Jilin Tan, Ping Liu, Shangli Wu, Yubao Meng, Qi Zhao, and Zhongyong Zhou, "System, method, and computer program product for input/output buffer modeling", U.S. Patent 9,460,250, issued October 4, 2016.
- Taranjit Kukal, Feras Al-Hawari, Dennis Nagle, Raymond Komow, and Jilin Tan, "System and method for implementing power integrity topology adapted for parametrically integrated environment", U.S. Patent 8,656,329, issued February 18, 2014.
- Feras Al-Hawari, Taranjit Kukal, Dennis Nagle, Raymond Komow, and Jilin Tan, "System and method for adapting behavioral models to fluctuations in parametrically integrated environment", U.S. Patent 8,452,582, issued May 28, 2013.
- Feras Al-Hawari, Jilin Tan, and Jose Schutt-Aine, "Method and system for adaptive modeling and simulation of lossy transmission lines", U.S. Patent 8,386,216, issued February 26, 2013.
- Taranjit Kukal, Feras Al-Hawari, Dennis Nagle, Raymond Komow, and Jilin Tan, "System and method for adapting electrical integrity analysis to parametrically integrated environment", U.S. Patent 8,286,110, issued October 9, 2012.
- Ambrish Varma and Feras Al-Hawari, "Method and system for screening nets in a post-layout Environment", U.S. Patent 8,060,852, issued November 11, 2011.

Best Paper:

- Robert Blake, Phil Murray, and Feras Al-Hawari, "Challenges in implementing DDR3 memory interface on PCB systems: A methodology for interfacing DDR3 SDRAM DIMM to an FPGA", CDNLIVE! EMEA, Silicon-Package-Board Co-design Track, Munich, Germany, May, 2008.

Journal Papers:

- Feras Al-Hawari, Omar Al-Sawaeer, Hala Barham, Omaymah Almashaleh, Rasha Al-Attal, Mahmoud Al-Sawwaq, Mohammad Hababbeh, and Mai Alshawabkeh, "A data-driven decision-support framework for supply management using multi-criteria evaluation and machine learning," International Journal of Information Management Data Insights, vol. 6, no. 2, Art. no. 100445, 2026.
- Feras Al-Hawari, Anoud Alufeishat, Mohammad Hababbeh, and Ahmad Alfalayleh, "Scrum-guided development of an intelligent payroll management system with rule-based automation and RAG chatbot support", Knowledge-Based Systems, Volume 347, 116301, 2026.
- Feras Al-Hawari, "Software design patterns for data management features in web-based information systems", Journal of King Saud University - Computer and Information Sciences, <https://doi.org/10.1016/j.jksuci.2022.10.003>, 2022.
- Feras Al-Hawari, Hala Barham, Omar Al-Sawaeer, Mai Alshawabkeh, Sahel Alouneh, Mohammad I Daoud, and Rami Alazrai, "Methods to achieve effective web-based learning management modules: MyGJU versus Moodle", PeerJ Computer Science, 7:e498, DOI:10.7717/peerj-cs.498, 2021.
- Feras Al-Hawari, Mohammed Al-Sammarraie, and Taha Al-Khaffaf, "Design, validation, and comparative analysis of a private bus location tracking information system", Journal of Advanced Transportation, 2020(8895927), pp. 1-18, 2020.
- Feras Al-Hawari, Mai Al-Zu'bi, Hala Barham, and Wael Sararhah. "The GJU website development process and best practices", Journal of Cases on Information Technology, IGI Global, 23(1), pp. 1-24, 2020.
- Feras Al-Hawari, "Holistic university website management: people, technology and processes", TEM Journal - Technology, Education, Management, Informatics, 9(4), pp. 1771-1779, 2020.
- Feras Al-Hawari and Mohammad Hababbeh. "Secure and robust web services for e-payment of tuition fees", International Journal of Engineering Research and Technology, 13(7), pp. 1795-1801, 2020.
- Rami Alazrai, Amal Al-Saqqaf, Feras Al-Hawari, Hisham Alwanni, and Mohammad I. Daoud. "A time-frequency distribution-based approach for decoding visually imagined objects using EEG signals", IEEE Access, Vol. 8, pp. 138955–138972, 2020.
- Daoud, M., Abdel-Rahman, S., Bdair, T., Al-Najar, M., Al-Hawari, F., and Alazrai, R., "Breast tumor classification in ultrasound images using combined deep and handcrafted features", Sensors, 20(23), pp.1-1, 2020.
- Feras Al-Hawari, Mahmoud Al-Ashi, Fares Abawi, and Sahel Alouneh. "A practical three-phase ILP approach for solving the examination timetabling problem", International Transactions in Operational Research, 27(2), pp. 924-944, 2020.
- Feras Al-Hawari. "Automatic and multithreaded method for determining the number of vector fitting poles based on empirical data", International Journal of Numerical Modelling Electronic Networks Devices and Fields, John Wiley, 32(2), e2512, 2019.
- Feras Al-Hawari, Mai Alshawabkeh, Haytham Althawbih, and Omar Abu Nawas. "Integrated and secure web-based examination management system", Computer Applications in Engineering Education, John Wiley, 27(4), pp. 994-1014, 2019.
- Feras Al-Hawari and Hala Barham. "A machine learning based help desk system for IT service management", Journal of King Saud University - Computer and Information Sciences, Elsevier, DOI: 10.1016/j.jksuci.2019.04.001, 2019.
- Sahel Alouneh, Feras Al-Hawari, Ismail Hababeh, and Gheorghita Ghinea. "An effective classification approach for big data security based on GMPLS/MPLS networks", Security and Communication Networks, Hindawi, vol. 2018, Article ID 8028960, 10 pages, 2018.

- Feras Al-Hawari, Anoud Alufieshat, Mai Alshawabkeh, Hala Barham, and Mohammad Hababbeh, "The software engineering of a three-tier web-based student information system (MyGJU)", *Computer Applications in Engineering Education*, 2(25), pp. 119-133, 2017.
- Feras Al-Hawari, "Analysis and design of an accounting information system", *International Research Journal of Electronics and Computer Engineering*, 3(2), pp. 16-21, 2017.
- Feras Al-Hawari, "MyGJU student view and its online and preventive registration flow", *International Journal of Applied Engineering Research (IJAER)*, 1(12), pp. 119-133, January 2017.
- Jose Schutt-Aine, Patrick Goh, Yidnekachew Mekonnen, Feras Al-Hawari, Jilin Tan, Ping Liu, and Wenliang Dai, "A comparative study of convolution and order reduction techniques for blackbox macro-modeling using scattering parameters", *IEEE Transactions on Components, Packaging and Manufacturing Technology (IEEE-TCPMT)*, 10(1), pp. 1642-1650, October 2011.
- Patrick Goh, Jose Schutt-Aine, Demetri Klokotov, Jilin Tan, Ping Liu, Wenliang Dai, and Feras Al-Hawari, "Partitioned latency insertion method with a generalized stability criteria", *IEEE Transactions on Components, Packaging and Manufacturing Technology (IEEE-TCPMT)*, 9(1), pp. 1447-1455, September 2011.

Conference Papers:

- Feras Al-Hawari, Khaled Tayem, Sahel Alouneh and Anass Al Ksasbeh, "Impact of Virtual Hadoop Cluster Scalability on The Performance of Big Data Mapreduce Applications," *2023 24th International Arab Conference on Information Technology (ACIT)*, IEEE, Ajman, United Arab Emirates, pp. 1-6, 2023.
- Feras Al-Hawari, Rawan Al-Twal, Hala Barham, Attaa Al-Khaleel and Sahel Alouneh, "Comparative Analysis and Graphic Design Elements to Enhance the Usability of a University Website," *2023 Tenth International Conference on Social Networks Analysis, Management and Security (SNAMS)*, Abu Dhabi, United Arab Emirates, pp. 1-8, 2023.
- Feras Al-Hawari, Khaled Tayem, Sahel Alouneh, and Anass Al-Ksasbeh, "Methodology to evaluate the performance of Hadoop MapReduce on a Hyper-V cluster using SAN storage", *The International Arab Conference on Information Technology (ACIT'2022)*, IEEE, Abu Dhabi, UAE, 2022.
- Sahel Alouneh, Ala' Khalifeh, Dhiah el Diehn I. Abou-Tair, and Feras Al-Hawari, "An open source LoRaWAN simulator framework for the Internet of Things applications", *8th International Conference on Internet of Things: Systems, Management and Security (IOTSMS)*, 2021.
- Feras Al-Hawari, Hadi Etaawi, and Sahel Alouneh, "A cost effective information display system based on open source technologies", *International Conference on New Trends in Computing Sciences (ICTCS 2017)*, pp. 277-282, Amman, Jordan, October 11-13, 2017.
- Feras Al-Hawari, "Analysis and design of an accounting information system", *7th International Research Conference on Science, management, and Engineering*, Dubai, UAE, 2017.
- Sahel Alouneh, Ismail Hababeh, Feras Al-Hawari, and Tamer Alajrami, "Innovative methodology for elevating big data analysis and security", *The 2nd International Conference on Open Source Software Computing (OSSCOM 2016)*, pp. 1-5, Beirut, Lebanon, December 1-3, 2016.
- Jose Schutt-Aine, Jilin Tan, Ping Liu, Feras Al-Hawari, and Ambrish Varma, "IBIS modeling using latency insertion method (LIM)", *16th IEEE Workshop on Signal Propagation and Interconnects (SPI)*, pp. 97-100, Sorrento, Italy, 13-16 May 2012.
- Patrick Goh, Jose Schutt-Aine, Demetri Klokotov, Feras Al-Hawari, Jilin Tan, Ping Liu, and Wenliang Dai, "Partitioned Latency Insertion Method (PLIM) with stability considerations", *15th IEEE Workshop on Signal Propagation and Interconnects (SPI)*, pp. 107-110, Italy, May 2011.
- Jose Schutt-Aine, Demetri Klokotov, Patrick Goh, Jilin Tan, Feras Al-Hawari, Ping Liu, and Wenliang Dai, "Application of the latency insertion method to circuits with blackbox macromodel representation", *11th IEEE Electronics Packaging Technology Conference (EPTC09)*, pp. 92-95, Singapore, December, 2009. (Invited Paper)
- Jose Schutt-Aine, Feras Al-Hawari, Jilin Tan, and C. Kumar, "Blackbox macromodel with S-parameters and fast convolution", *IEEE Workshop on Signal Propagation and Interconnects (SPI-08)*, pp. 1-4, Avignon, France, May 2008.

- Feras Al-Hawari, "S-parameter based multi-conductor transmission line modeling and simulation", Cadence Technical Conference, Anaheim, California, May 2008.
- Phil Murray and Feras Al-Hawari, "Challenges in implementing DDR3 memory interface on PCB systems: a methodology for interfacing DDR3 SDRAM DIMM to an FPGA", DesignCon 2008, Santa Clara, California, February 2008.
- Feras Al-Hawari, "Fast time domain analysis of frequency dependent data using the direct convolution with approximation approach", Cadence Technical Conference, Monterey, California, April 2005.
- Feras Al-Hawari and Jilin Tan, "S-parameter based wideband simulation technology on digital circuit boards", Cadence Technical Conference, San Jose, California, May 2003.
- C. Kumar and Feras Al-Hawari, "Template oriented software design", Cadence Technical Conference, Napa Valley, California, May 1996.

Demonstrations:

- Kent Drumstad, Adge Hawes, Taranjit Kukal, Feras Al-Hawari, Ambrish Varma, and Terry Jernberg, "Supporting external circuit as spice or s-parameters in conjunction with I-V/V-T tables", Asian IBIS Summit, Yokohama, Japan, November 2011.
- Feras Al-Hawari, "Setup and analysis of DDR2 source synchronous memory interfaces in Allegro PCB SI", Cadence Technical Conference, Keystone, Colorado, May 2007.
- Feras Al-Hawari, "A demo for s-parameters transient simulation support in SigXP", Cadence Technical Conference, San Jose, California, April 2004.

Posters:

- Elias Manolakos, Demetris Galatopoulos, and Feras Al-Hawari, "MATLAB and Java integration for distributed image processing applications", Communications and Digital Signal Processing Center, Northeastern University, March 2008.
- Feras Al-Hawari, "A method for SPICE-level transient simulation of digital PCB structures characterized by S-parameters", Cadence Technical Conference, San Jose, California, April 2004.

White Papers:

- Feras Al-Hawari and Elias Manolakos, "Application-aware middleware to support runtime component self-adaptation strategies in cluster computing", Electrical and Computer Engineering Department, Northeastern University, Boston, USA, 2008.
- Feras Al-Hawari and Elias Manolakos, "Middleware to support self-adaptation of components for fault tolerance in network computing applications," Electrical and Computer Engineering Department, Northeastern University, Boston, USA, 2008.
- Feras Al-Hawari and Elias Manolakos, "Startup-phase QoS management system and an efficient mapping heuristic for network computing applications", Electrical and Computer Engineering Department, Northeastern University, Boston, USA, April 2006.
- Feras Al-Hawari and Elias Manolakos, "Performance engineering of coarse grain network computing applications", Electrical and Computer Engineering Department, Northeastern University, Boston, USA, April 2005.

Other Publications:

- Feras Al-Hawari, "Help: JavaPorts Visual Task Composer (JPVTC)", Electrical and Computer Engineering Department, Northeastern University, Boston, MA, 2006.
- Feras Al-Hawari, "Help: QoS GUI", Electrical and Computer Engineering Department, Northeastern University, Boston, MA, 2006.
- Feras Al-Hawari, "Help: QoS service and middleware for runtime adaptation and application fault tolerance", Electrical and Computer Engineering Department, Northeastern University, Boston, 2006.
- Feras Al-Hawari, "Tutorial: constructing network application models using JavaPorts tools", Electrical and Computer Engineering Department, Northeastern University, Boston, MA, 2006.

Capacity Building Projects

- *International Master of Science on Cyber Physical Systems (MS@CPS)*. GJU Investigators: Dhiah Abou Tair, Sahel Alouneh, Ala Khalifeh, Samer Nofal, and Feras Al-Hawari. Erasmus+ program - Key Action 2 - Capacity Building in the Field of Higher Education, European Commission. Period: 1/11/2018-31/10/2021.
- *Jordan Opportunity for Virtual Innovative Teaching and Learning (JOVITAL)*. GJU Investigators: Dr. Mohammad Daoud, Dr. Sahel Alouneh, Dr. Rami Alazrai, and Dr. Feras Al-Hawari. Erasmus+ program - Key Action 2 - Capacity Building in the Field of Higher Education, European Commission.
- *A Bottom-up Approach for Opening up Education in South-Mediterranean Countries (OpenMEd)*. GJU Investigators: Mohammad Daoud, Manar Fayyad, Salem Al-Agtash, Loay Salhie, Rana Sabri, Sahel Alouneh, and Feras Al-Hawari. Erasmus+ program - Key Action 2 - Capacity Building in the Field of Higher Education, European Commission. Period: 1/10/2015-30/9/2018.

Awards

- **The German Jordanian University Award of Excellence** (2016) for establishing the software development team, architecting the student information, accounting, and financial systems, and contributing directly to their development.

Courses Taught

- Computing Fundamentals and Lab
- Object Oriented Programming and Lab
- Systems Programming and Lab
- Software Design and Architecture
- Advanced Software Analysis and Design
- Digital Systems Lab
- Operating Systems Lab
- Parallel Architectures and Parallel Algorithms
- Parallel and Distributed Computing
- Electrical Circuits I and II
- Electrical Circuits Lab
- Senior Project I and II
- Master's Thesis (Supervisor)

University and External Committees and Governance

- Member, GJU Deans Council
- Chair, SEEIT School Council
- Chair, SEEIT Research Council
- Chair, SEEIT Graduate Studies Council
- Chair, SEEIT Dual Studies Committee
- Chair, SEEIT Marketing Committee
- Member, University Dual Studies Committee
- Member, Dual Studies Revision Committee
- Member, Registration Procedures Committee
- Member, Admission Requirements Committee
- Member, Employee Affairs Committee

- Member, Committee for Reviewing Study Plans of New B.Sc. Programs at GJU
- Member, GJU Staff Mobility Program (SMP) Selection Committee
- Member, Technical Advisory Committee, Jordanian Universities Network (JUNET)
- Member, University Emergency Committee
- Member, MOHE E-Learning Committee
- Member, MOHE Priorities Implementation Committee
- Member, Digital Teaching Strategy Steering Committee
- Chair, Digital Teaching Strategy Technical Committee
- Member, Coronavirus Committee
- Member, Online Examination Guidelines Committee
- Member, University Directors Committee
- Member, E-Learning Committee
- Member, Similar Courses Committee
- Member, Student Elections Committee
- Member, Central Tenders Committee
- Member, Student Disciplinary Board
- Member, Inventory and Stocking Committee
- Member, University Budget Committee
- Member, ERP Tools Evaluation Committee
- Member, Quality Assurance and Accreditation Committee
- Member, Data Center Migration Committee
- Member, Project Acceptance Committees for Network Infrastructure, IP Video Surveillance, the Data Center, Video Conferencing Systems, and Smart Classrooms
- Member, Computer Engineering Department Graduate Studies Committee
- Member, Computer Engineering Department Scientific Research Committee
- Member, M.Sc. in Computer Engineering Comprehensive Examination Committee
- Member, M.Sc. Thesis and Senior Project Defense Committees

ERP Development and Digital Transformation Leadership

German Jordanian University | 2013–Present

- **Founded and built GJU's in-house software development capability**, entrusted by the University President and Deans Council to establish the team, technology foundation, and delivery practices for the university's ERP systems and portal. Have continuously led its evolution from the Information Systems and Technology Center in 2013 to the separate Computerization Project in 2021 and the Digital Transformation Office in early 2025.
- **Built and trained a multidisciplinary team, now comprising 13 members, and continue to lead its projects and technical direction.** The team includes nine software engineers responsible for systems analysis and Java EE development, a database administrator, a quality assurance specialist, a website administrator/developer, under my project and technical leadership. Developed the team's expertise through training in enterprise application development, software architecture, design patterns, and database analysis and design.
- **Architected the ERP and university portal ecosystem and personally developed major core components for registration, revenue, payroll, HR, and supplies management.** Established the three-tier Java EE and Oracle architecture, standardized project structures, reusable templates, design patterns, engineering guidelines, and in-house Git version control. Also oversee the Drupal university website and Moodle e-learning platform, with PostgreSQL supporting Moodle.

- **Lead the university's digital transformation agenda and project portfolio**, translating stakeholder requirements into initiatives prioritized with university management. Directing analysis, design, development, quality assurance, functional/stress testing, and deployment. Providing technical guidance on complex implementation challenges and algorithm design. Established Agile Scrum delivery processes incorporating selected ISO/IEC 29110 project management and software engineering practices.
- **Direct application operations and production releases**, administering application servers, monitoring server health and logs, and validating and deploying updates. Participate in database administration and execute schema and data changes required for application releases.
- **Established infrastructure and operational controls in coordination with IT**, covering Hyper-V virtualization, Oracle Linux server configuration, and staging environments. Defined administrative access roles and responsibilities for system administration, database administration, and cybersecurity. Established security policies, upgrade procedures, and multi-tier backups.
- **Extended the program's impact through research and institutional adoption**, published research on university systems, predominantly in leading journals, with additional conference publications. Led the development of user documentation, written and video tutorials, and employee training to support effective system use across the university.

Selected Systems and Platforms

University systems delivered under my architectural and project leadership, with direct development contributions to core ERP components.

- **MyGJU Integrated University Portal:** Role-based gateway connecting academic and administrative services across the university. Supports registration, academic and financial records, grading, advising, e-learning, and workflows for German Year study and internships, course substitutions, seat reservations, and study postponement. Provides employee profiles, salary slips, fund accounts, supplies, and help desk services, with requests and approvals for vacations, leave, incentives, conference participation, and sabbaticals. Coordinates student and employee clearance and departmental review of job applications. Leadership dashboards and extensive reporting support institutional oversight and decision-making.
- **Student Information System:** Registrar platform managing the student lifecycle from admission through graduation. Covers academic structures, study plans, registration, student records, transfer credit, grades, GPA and academic standing, graduation eligibility, certificates, and reporting. Connects academic operations with HR through shared organizational and instructor records, administrative roles, and workload reporting, while linking registration with student accounting. Delivers academic information and services through MyGJU and supports registrar approvals and record updates across student workflows, including course substitutions, study postponement, German Year credit equivalency, and clearance.
- **Financial Management, Student Accounting, and Electronic Payments:** Connects institutional budget management, student accounting, and electronic collections. Supports budget allocations, adjustments, transfers, cost centers, procurement commitments, vouchers, and financial reporting. Manages tuition and service fees, scholarships, sponsorships, invoices, payments, refunds, account statements, and semester financial closing. Links E-Fawateercom payments directly to accounting records using official university IDs and assigned external-user identifiers.
- **Human Resources and Payroll:** Integrates organizational administration, employee management, recruitment, and automated payroll. Supports university structures, employee profiles, appointments, promotions, benefits, training, and personnel archives. Links departmental vacancy requests through MyGJU with HR review, publication, and application routing for departmental assessment. Connects MyGJU requests and approvals with HR processing for vacations, leave, academic workloads, and clearance. Uses employee records and configurable payroll rules to calculate salaries, allowances, deductions, taxes, insurance, and social security contributions. Generates detailed pay-slips and tax statements, supports retroactive adjustments, and provides HR and payroll reporting and audit controls.
- **Supplies Management:** Manages the full supplies lifecycle from planning and requests through procurement, receiving, warehousing, inventory control, custody, issuance, returns, and disposal. Coordinates role-based workflows, approvals, documentation, and reporting, linking operations with financial commitments, accounting records, and employee information. Provides employee self-service through MyGJU for requests, item exchanges, and access to custody records.

- **MyGJU Guests External Services Portal:** Portal for prospective students and other external users to submit admission and job applications and register for training courses. Collects applicant information and supporting documents for review and processing by the responsible university units. Assigns each user a unique identifier for electronic payments through E-Fawateercom.
- **Help Desk, Electronic Correspondence, and Document Archiving:** Platform providing university units with service request management, paperless internal correspondence, and document archiving. Help Desk Admin enables unit administrators and managers to configure roles and services and manage tickets. Users submit and track service requests through MyGJU. Automated routing, notifications, and tracked response requests support correspondence workflows within and between units. Detailed ticket metadata enables organized archiving and rapid document retrieval. Management dashboards track ticket progress, closure, and service performance to support oversight and decision-making.
- **Digital Learning, Website, and Campus Communication:** Moodle e-learning platform and an online examination system supporting exam authoring, scheduling, automated grading, reporting, and authentication controls. Includes the Drupal university website and centrally managed digital signage for campus announcements, news, and multimedia.

Technology Stack: Java / Java EE, Oracle Database, PostgreSQL, JSF, PrimeFaces, JavaScript, HTML/CSS, GlassFish, Drupal, Moodle, Hyper-V, Oracle Linux, Git.

Emergency COVID-19 Transition & Online Education Infrastructure (GJU)

In response to the coronavirus crisis, Dr. Al-Hawari led the Information Systems and Technology Center (ISTC) team through intensive 24/7 operations to maintain total institutional continuity, enabling fully online teaching, assessment, and administration during the second semester of the 2019/2020 academic year and laying the foundation for hybrid learning infrastructure. Key initiatives and measures included:

- **Platform Architecture & Tech Stack Selection:** Evaluated Microsoft Office 365 tools, deployed enterprise-wide by ISTC since 2017, to architect a secure, robust remote-learning ecosystem. Standardized solutions included MS Teams for interactive lecture streaming and recording, Skype for Business for video conferencing, MS Stream for video archiving, Moodle LMS for electronic assessments, MyGJU for course portfolios, attendance, and grading, OneDrive and Outlook for storage and communications, and MS Office / Whiteboard for digital authoring.
- **Hardware Standardization & Smart Classrooms:** Established technical specifications for all remote-learning hardware (desktops, laptops, tablets, specialized microphones, webcams, and printers). Formulated hardware and software requirements for 15 smart classrooms designed to support interactive online and hybrid learning, overseeing procurement and successful deployment in 2021.
- **Faculty Enablement & Video Tutorials:** Launched dedicated e-learning website pages and partnered with the university's e-learning committee to produce comprehensive video tutorials covering supported platforms, remote teaching workflows, and multi-format online examination methodologies (including handwritten/typewritten submissions, electronic multiple-choice tests, and structured oral exams).
- **High-Availability Moodle Assessment Infrastructure:** Configured, fine-tuned, secured, and load-tested Moodle servers to reliably support over 1,000 concurrent users during high-stakes university quizzes and examinations, backed by round-the-clock technical troubleshooting and live support.
- **Administrative Continuity & E-Signatures:** Deployed an enterprise electronic signature service enabling faculty and staff to securely sign documents online, ensuring uninterrupted institutional governance and administrative workflows.
- **24/7 Helpdesk & Continuous Feedback Loops:** Provided round-the-clock technical support for faculty and students regarding user accounts, platform usability, and exam troubleshooting. Organized structured webinars in coordination with the e-learning committee to solicit faculty feedback, evaluate remote teaching experiences, and iteratively refine institutional digital service.

Industry Collaboration and Professional Service in the USA

- **Associate Editor**, *IEEE Transactions on Components, Packaging and Manufacturing Technology* (2012–Present).
- **Member**, **IBIS Advanced Technology Modeling Task Group**, contributing to the development and promotion of advanced electronic-interface modeling, with an emphasis on SerDes-based designs (2009–2012).
- **Lead Researcher**, **Cadence–University of Illinois at Urbana-Champaign Collaboration**, working with Prof. Jose E. Schutt-Aine on transient simulation techniques and model order reduction for passive and nonlinear circuits (2005–2012).
- **Industry Collaboration with Micron, Altera, and Celestica**, jointly architecting signal integrity analysis workflows for source-synchronous memory interfaces, including DDR2 and DDR3, in Allegro PCB SI (2005–2012).
- **Cadence–IBM Integration Project**, contributing to the integration of IBM tools, including the PowerSpice simulator and CZ2D field solver, into Allegro Package/PCB SI (2006).
- **Cadence–Intel Research Project**, contributing to efficient transient simulation methods for passive structures characterized by S-parameters (2002).
- **Technical Program Committee Member**, Cadence Technical Conference, California (2006).
- **Technical Consultant** on applications and methodologies related to SpecctraQuest and SigXP (2000–2012).

Research and Development at Cadence Design Systems

17 years of experience across the software development lifecycle, spanning product requirements, functional and design specifications, development, testing, and maintenance.

Circuit Simulation Technology

- Served as technical lead for circuit simulation technology within the Silicon/Package/Board (SPB) High Speed group, maintaining and advancing Tlsim, the SPICE-based engine used in Allegro Package/PCB SI for AC, DC, and transient analysis. Helped define the future direction of the group's simulation technologies.
- Implemented three methods for modeling and transient simulation of passive structures characterized by frequency-dependent Z, Y, and S parameters:
 - **Direct convolution:** Derived impulse responses using IFFT and applied convolution to calculate time-domain port currents and voltages. Enforced model passivity and response causality using the Hilbert transform.
 - **Fast convolution:** Implemented accelerated convolution to improve transient simulation performance.
 - **Macro-modeling:** Used vector fitting to derive pole-residue models and corresponding time-domain formulations for efficient transient circuit simulation.
- Developed transient simulation methods for transmission lines characterized by frequency-dependent RLGC data, combining split S-parameters, delay extraction, vector fitting, partial-fraction representations, and state-space formulations.
- Investigated the Latency Insertion Method (LIM) for fast transient simulation.
- Maintained and enhanced transient simulation support for nonlinear IBIS models, W-element transmission lines, diodes, voltage- and current-controlled sources, and lumped R, L, C, and K elements.
- Maintained the SPICE parser, matrix package, and waveform-generation code.
- Integrated Intel Math Kernel Library (MKL) into Tlsim to enable automatic parallelization of matrix algorithms on multicore processors.

Source-Synchronous Interface Analysis

- Led five engineers in architecting and developing a post-route analysis flow for source-synchronous interfaces, including double data rate (DDR) memory interfaces, in Allegro PCB SI (SpecctraQuest). The flow supported:
 - **Interface configuration:** Controller and SDRAM identification; data, address, and control bus definition; strobe and clock association; pseudorandom bit-pattern assignment; and programmable on-die termination (ODT) settings for driving, receiving, and standby modes.

- **Analysis and simulation:** Reflection, crosstalk, and simultaneous switching noise (SSN), with automated simulation across ODT settings, driver and receiver combinations, and I/O buffer process, voltage, and temperature (PVT) variations.
- **Measurements and reporting:** Worst-case setup and hold times and margins, noise margins, overshoot, undershoot, and eye diagrams. Incorporated timing adjustments based on measured data and clock slew rates and user-defined derating tables.

Simulation Frameworks and Circuit Construction

- Designed and implemented an open framework for third-party simulation engines, including HSPICE, Spectre, and PowerSpice, within Cadence's pre- and post-route Allegro PCB SI tools, including SigXplorer and SpectraQuest. Developed the GUI, model templates, infrastructure, netlist and waveform translators, measurement capabilities, and reporting. Enabled simulation with complex structural and transistor-level I/O models beyond behavioral IBIS representations, supporting concurrent IC and PCB design. The architecture was subsequently extended to accommodate third-party engines such as 2D and 3D field solvers.
- Maintained and enhanced the SpectraQuest circuit builder, generating SPICE netlists for selected PCB nets. Integrated driver and receiver models from device libraries, field-solver models for traces and vias, and analysis-specific stimuli for reflection, crosstalk, and SSN.
- Contributed to the S-parameter generation flow in SigXplorer, using AC frequency sweeps to create black-box models of passive topologies containing transmission lines, S-parameter models, vias, capacitors, resistors, and mutual inductors.
- Developed and enhanced waveform measurement and reporting code for switching, settling, setup and hold times, overshoot, and noise margins. Stored results in the internal simulation cache for summary reporting.

Model Libraries and Data Integration

- Designed GUIs, data structures, and C/SKILL database APIs for the device modeling library (DML) and interconnect modeling library (IML) in SpectraQuest.
- Developed a geometry-comparison API for IML models, enabling the circuit builder to reuse previously solved trace and via models. Invoked the field solver and cached new models when no matching geometry was available.
- Implemented storage of device models in the Allegro database and a GUI for comparing and synchronizing those models with the DML library.
- Developed and maintained model and netlist translators, including:
 - **ibis2signoise:** IBIS to DML conversion.
 - **spc2spc:** Tlsim netlist conversion to HSPICE or Spectre.
 - **ts2dml:** Touchstone to DML conversion.
 - **dmlcheck:** DML syntax checking and model validation.
- Implemented a GUI for invoking s2ibis, converting transistor-level SPICE I/O models into behavioral IBIS models represented by I/V and V/t curves.
- Worked with SWATH connectors, packaged devices, and electrical board description (EBD) models.

Engineering Utilities, Testing, and Portability

- Developed design/net audit utilities to verify PCB and net configuration for signal integrity analysis.
- Implemented an MFC application for displaying stripline and microstrip transmission lines.
- Developed C-shell regression scripts for delivered features and tools.
- Ported simulator and circuit-builder code from UNIX to Windows.

Ph.D. Dissertation Research: Application-Level QoS Management for Heterogeneous Network Computing

Dr. Feras Al-Hawari conducted his Ph.D. research at Northeastern University under the supervision of Prof. Elias Manolakis, contributing to JavaPorts, a distributed, component-based framework for heterogeneous network computing. He designed and developed an application-level Quality of Service (QoS) management system comprising two complementary frameworks:

1) Startup-Phase QoS Management Framework

Automate task mapping of network computing applications onto Networks of Workstations (NOWs) prior to launch.

- **Interactive QoS GUI & Management Framework:** Developed an interactive graphical user interface and underlying framework enabling developers to run QoS management sessions to rapidly identify optimal task-to-machine mappings that satisfy target performance metrics (e.g., total execution time or speedup ratio) at startup. The framework utilizes efficient mapping heuristics and performance estimation algorithms, while the GUI serves to define machine pools, deploy/terminate resource monitoring modules, and display real-time resource data.
- **Scalable & Non-Intrusive Resource Monitoring System:** Engineered a scalable, ring-configured monitoring architecture using JavaPorts messaging to periodically measure static and dynamic machine attributes (CPU count, frequency, workload, free swap/RAM, domain name, OS type) and network link performance. Measures application-level (RMI) and network-level (TCP/IP) throughput and latency using multi-size message probing to predict throughput for any payload size, coordinating monitoring events via a token-passing mechanism across logical ring links.
- **JavaPorts Visual Task Composer (JPVTC):** Created a visual modeling tool that enables developers to construct behavioral task graphs and build complete, two-level hierarchical network computing application models for performance engineering and rapid prototyping prior to code development. The tool models core code constructs, sequential blocks, iteration loops, conditionals, synchronous/asynchronous read/write message passing, and thread spawning, and serializes behavioral task graphs into an XML format defined by a graph Document Type Definition (DTD).
- **Efficient Mapping Heuristics:** Formulated advanced mapping algorithms to allocate compute- and communication-intensive, multi-tasked distributed applications to the best available resources based on network representations, application models, and static/dynamic resource states.
- **Simulation-Based Performance Estimation Scheme:** Designed a simulation engine leveraging JPVTC application models and dynamic resource states to accurately predict total execution times. The scheme accounts for execution, queuing, and synchronization delays and detects potential deadlocks by simulating a time-sliced CPU scheduler (queuing contending tasks/threads) and mimicking JavaPorts communication port lists.
- **Network Clustering Algorithm:** Implemented a clustering methodology to group machines with similar communication profiles into a unified cluster graph, representing the network as a simplified, fully connected graph to drastically reduce the intra- and inter-cluster throughput measurements needed for all-to-all communication estimation.

2) Runtime QoS Service & Middleware

Facilitate runtime self-adaptation driven by the application for performance optimization (e.g., load balancing) and fault tolerance (e.g., overcoming machine and task crashes).

- **Lightweight Adaptive Middleware:** Designed a tightly coupled runtime middleware that launches and terminates automatically alongside the companion network computing application. Configured based on application task structure to run only necessary monitors, it tracks dynamic task and resource states (detecting machine/task crashes for fault tolerance) and monitors CPU speed, workload, RAM, and network link throughput to route jobs and messages to optimal compute and network resources.
- **Resource-Independent Anonymous API:** Architected a simple, anonymous API enabling tasks to query views of measured attributes across monitored entities (tasks, machines, links) to drive intelligent self-adaptation decisions. Because destination names and ports are omitted from API methods, application code remains completely independent of underlying physical resources, enabling seamless execution on new machine pools without code modifications. Additionally, it supports dynamic runtime control methods allowing tasks to halt, resume, or modify monitoring behavior on-the-fly to eliminate overhead when resource tracking is temporarily unneeded.

Computer Skills

- **Programming Languages and Software Design:** Java SE/EE, C, C#, C++, Python, Ada, Pascal, Fortran, SKILL, MATLAB, assembly languages, object-oriented analysis and design (OOA/OOD)
- **GUI and Web-Interface Development:** Java Swing, Visual C#, Visual C++, JSF, JSP, PrimeFaces
- **Cloud Deployment and Server Administration:** AWS LightSail, Amazon Linux, Amazon Corretto JDK, GlassFish, and PostgreSQL, including application deployment, network and firewall configuration, port management, and secure SSH access
- **Java Development and Deployment:** Java JDK, Maven, Apache NetBeans, Eclipse GlassFish, and PostgreSQL
- **Parallel and High-Performance Computing:** CUDA GPU programming, MPI distributed-memory parallelism, OpenMP shared-memory programming, and Linux virtual cluster setup using VirtualBox for teaching
- **Python Development and Data Analytics:** Spyder, Conda, NumPy, pandas, and Matplotlib for data processing, analysis, and visualization
- **Machine Learning:** Regression, classification, K-means clustering, model training, and performance evaluation
- **Machine Learning Applications:** IT ticket classification, supplier performance assessment, budget forecasting, budget-spending analysis, and employee-performance analysis
- **Generative AI and AI-Assisted Development:** RAG chatbot development using LangChain, FAISS, and Hugging Face APIs, including document chunking, embeddings, retrieval, and LLM/RAG ablation testing. OpenAI Codex for coding assistance
- **Network and Distributed-Programming APIs:** Java and C TCP/IP APIs, Java Remote Method Invocation (RMI)
- **Networking Models and Protocols:** OSI reference model, Ethernet, Asynchronous Transfer Mode (ATM), SONET, TCP/IP, OSPF, and IGRP
- **Hardware Description Languages:** VHDL
- **Scripting and Web Languages:** C shell, JavaScript, and PHP
- **Database Technologies and Design:** SQL, JDBC, ADO.NET, Oracle, PostgreSQL, MySQL, Microsoft SQL Server, Microsoft Access, entity-relationship modelling, fact-based database analysis, and database normalization
- **Database Administration and Development Tools:** Oracle SQL Developer, MySQL Administrator, SQL Server Configuration Manager, Navicat Lite for MySQL, MySQL Workbench, SQL Server Management Studio, and Microsoft Access
- **Java Security Technologies:** Java Cryptography Architecture (JCA), Java Secure Socket Extension (JSSE), Java Authentication and Authorization Service (JAAS), and Java keytool
- **Operating Systems and Development Platforms:** Windows, UNIX, Linux, HP platforms, AIX, MS-DOS, and VAX/VMS
- **Development and Debugging Tools:** Visual C++.NET, Visual C#.NET, Workshop, Visual Studio C++, NetBeans IDE, Forte for Java, dbx, Purify, and Quantify
- **Application and Web Servers:** Apache and GlassFish
- **Circuit Simulators:** Tlsim, HSPICE, PSpice, Spectre, and SPICE3
- **PCB, IC, and EDA Design Tools:** Cadence Allegro Package/PCB SI tools, including SpectraQuest, SigXplorer, Power Integrity, Model Integrity, Constraint Manager, SigWave, Allegro Router, and Advanced Package Designer, Cadence IC tools, Agilent ADS tools, SUPREM, and VHDL tools
- **Documentation and Productivity Tools:** Microsoft Word, Microsoft PowerPoint, Microsoft Excel, LaTeX/TeX, FrameMaker, EndNote, Visio, Xfig, and vi
- **Version Control and Development Utilities:** Git, ClearCase, SourceTree, Cygwin, Lex/Yacc, and FrontPage
- **Additional Technical Skills:** C# and Java multithreading and collections, XML, DTD, DHTML, USB specification, AMPL, SHARPE, Petri Net tools, Spice2IBIS

Supervised University Projects

- **Enterprise Database Management & Administration Utility:** Engineered a lightweight, full-featured database administration tool (comparable to Navicat and MySQL Administrator) using Java (Swing/AWT) and JDBC to connect, query, and manage user and system databases within MySQL RDBMS environments.
- **National Geographic & Spatial Reference Database:** Developed, populated, and managed a centralized relational reference database housing over 41,000 verified U.S. ZIP code, city, and state tuples for seamless cross-system referencing.
- **VLSI & Integrated Circuit Design:** Executed full-custom IC design cycles using Cadence IC tools spanning schematic capture, Design Rule Check (DRC), routing, simulation, and verification. Modeled deep submicron CMOS transistor characteristics using SUPREM and designed complex analog/digital electronic circuits (differential amplifiers, I/O buffers, rectifiers, and oscillators) via PSPICE.
- **Hardware Description & Digital Systems Architecture:** Implemented structural and behavioral hardware designs, including complete CPU architectures, RAM modules, ALUs, and complex sequential/combinational circuits, utilizing VHDL.
- **Microprocessor Interfacing & Embedded Firmware:** Designed, built, and tested custom Motorola 68000 microcomputer systems, integrating hardware peripherals including monitors, printers, seven-segment displays, RS-232 serial interfaces, and closed-loop temperature/speed control modules programmed in low-level assembly. Developed a custom 6809 assembler.
- **Network Simulation:** Engineered a custom 8-node network simulation tool modeling packet transmission across physical, data link, and network layers.
- **Distributed Computing:** Implemented and benchmarked static and dynamic mapping heuristics (including Opportunistic Load Balancing [OLB], Minimum Completion Time [MCT], and K-Percent Best [KPB]) for scheduling independent tasks in heterogeneous computing (HC) environments using Request (self-scheduling) and Manager-Worker paradigms.